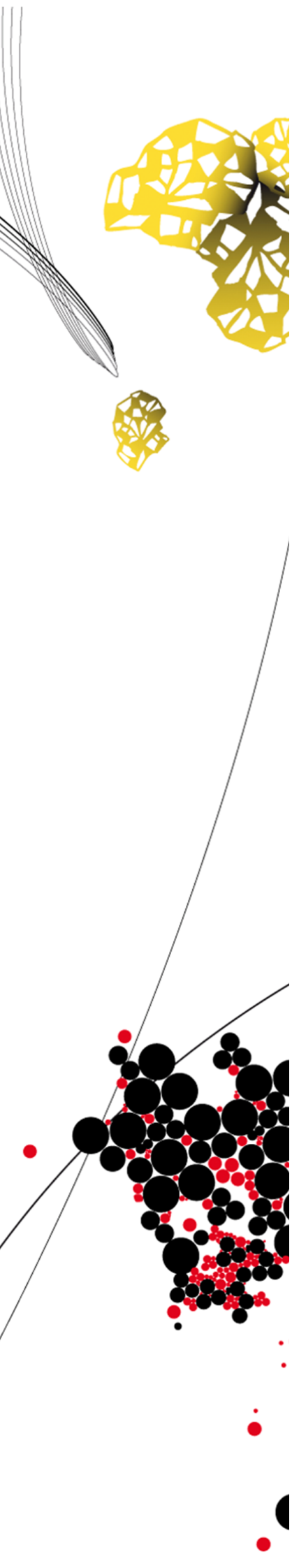

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Feasibility Study of Frequency Doubling using a Dual-Edge Method

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MSc. Thesis
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Abstract

The performance of integrated Frequency Synthesizers relies on a clean fixed reference frequency, which is usually derived from a crystal. Unfortunately, commercially cheap crystal oscillators are limited in the range from 20 - 50 MHz. In general, a higher reference frequency results in better noise performances for Frequency Synthesizers. Therefore it is desired to be able to double the reference frequency and at the same time preserving the clean crystal properties.

This work examines the feasibility of a low power and low noise CMOS Frequency Doubler in CMOS IC-technology. Main target specifications are: -151 dBc/Hz phase-noise floor, 10 kHz flicker noise corner frequency and reference spurs at the synthesizer output should be smaller than -80 dBc, within a power budget of approximately 4 mW. Within this scope a Phase-Locked Loop (PLL) has been analyzed, which showed insufficient yield for successful realization of a frequency doubler that would meet the given demands.

Next to a PLL, an alternative has been examined which relies on passing through the edges of the clean reference crystal. By combining both rising- and falling edges of the reference frequency (f_{ref}) into both rising edges, an output frequency of 2 x f_{ref} is obtained. Main drawback of this approach is static timing errors between adjacent periods that result from even-order distortion or duty-cycle error of the incoming reference frequency. This has been overcome by detecting the error and correcting it by means of a control loop. The system has been analyzed on system level, its behavior quantified, and implemented on circuit level.

Contents

Chapter 1

Introduction

Wireless communication takes in an increasingly important role in our everyday lives. Mobile phones for example, took a flight from voice communication since its introduction mid eighties to broadband internet access today. Much of the functional complexity of such a Radio Frequency (RF) device is carried out by digital circuitry in the low-frequency baseband range. Along with digital signal processing, the analog circuitry is an essential part of the hardware since this is operating in the RF range to mix these signals to baseband to be able to convert them to digital signals [Fig. 1.1].

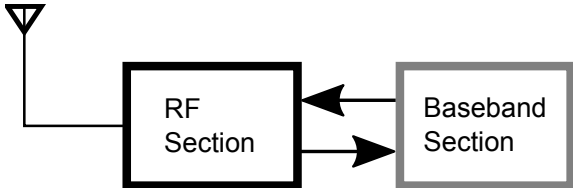


Figure 1.1: RF and baseband sections in an RF device.

An example of an RF section can be a radio-frequency receiver, where a stable[1] frequency is used to tune to a radio-frequency of interest. In nowadays Integrated Circuits (IC) this is done by integrating a frequency synthesizer to generate a variety of stable tunable frequencies. A frequency synthesizer relies on a clean fixed reference frequency which is usually derived from a crystal and determines for a big part the performance of the frequency synthesizer.

Unfortunately, commercially cheap crystals are limited in the range of 20 - 50 MHz. For a fractional-N synthesizer, a higher reference frequency allows to reduce the noise contribution from the sigma-delta modulator in the fractional-N synthesizer. Therefore there is the desire to double (or even better, multiply) the reference frequency and at the same time preserving the clean crystal properties.

[1]Stability is usually defined as long-term stable and short-term stable. The first defines its stability over a longer period of time which ensures absolute accuracy. The second defines its spectral purity in terms of phase noise and jitter which is important to prevent down-mixing of unwanted interferer signals.

1.1 Project Goal

The goal of the project is to examine the feasibility of a low power and low noise solution for a sub-section between the fixed reference frequency (crystal) and the frequency synthesizer, with the purpose of frequency doubling (Fig. 1.2).

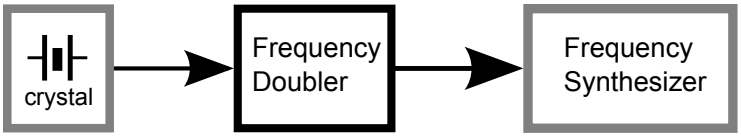


Figure 1.2: System perspective of doubler sub-section.

1.2 Specifications

Since the frequency doubler[Fig.1.2] will act as the fixed reference frequency for the frequency synthesizer, it is not hard to imagine that the frequency doubler is not allowed to deteriorate too much in terms of noise properties compared to the crystal. This puts relatively high demands on the doubler sub-section since a crystal oscillator has naturally very good noise properties.

The input frequency, that is the clean crystal reference frequency, is assumed to range from 20 to 50 MHz (the range in which crystals are still commercially available cheaply). Based on synthesizer specifications, Catena derived requirements for the frequency doubler as illustrated in Fig. 1.3 and given in Table

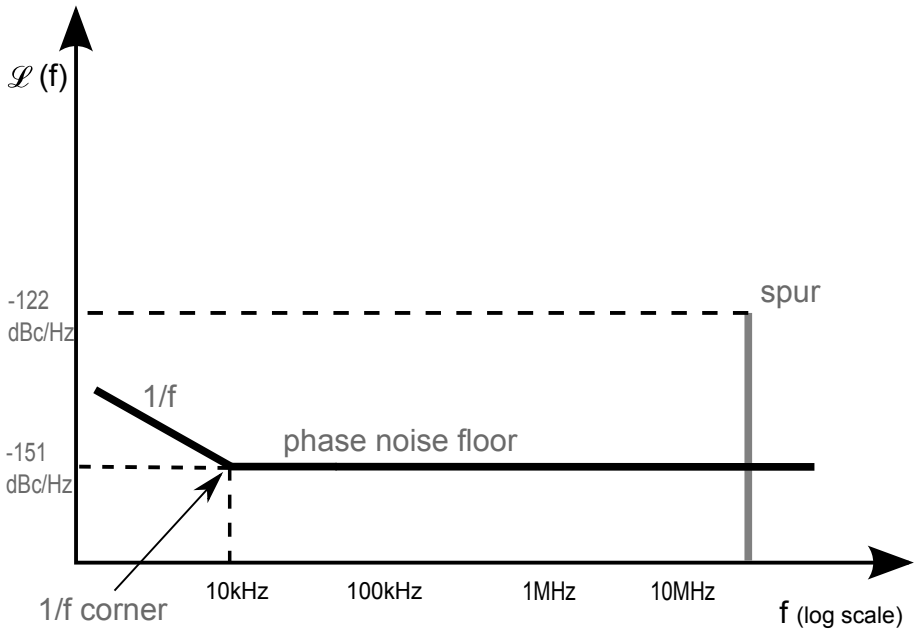


Figure 1.3: Specifications overview.

1.1. The doubled output frequency, thus in the range of 40 - 100 MHz, has a noise floor of -151 dBc/Hz. The 1/f corner frequency, which is usually dominated by the flicker noise of MOSFETS for in example buffers, should not exceed 10 kHz. Furthermore are spurious tones in the frequency spectrum are not allowed to be greater than -122 dBc. These specifications have to be met within a power budget of roughly 4 mW .

Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Output frequency		$2 \cdot f_{in}$		Hz
Output phase noise floor		-151	-149	dBc/Hz
Output phase noise 1/f corner		10k	15k	Hz
Output spurious			-122	dBc
Power dissipation		4m		Watt

Table 1.1: Target performance specifications.

1.3 Solution Directions and State-of-the-Art

This document first examines the feasibility of realizing a frequency doubler with the given specifications by means of Phase Locked Loop (PLL).

Next to a PLL, an alternative method that exploits both already available crystal edges is explored. The latter method has been used in front of the $\Sigma\Delta$ frac-N frequency synthesizer in [1] to reduce the in-band phase noise. The paper describes that both edges are combined by means of a delay element and an XOR gate, which is more recently also reported in [2]. Although [1] does not give extensive analysis and performance of the doubler circuit, it does report the need for a correction circuit to deal with the duty-cycle error that will lead to reference spurs. The duty-cycle correction (DCC) circuit as proposed in [1] is a digital solution with a resolution of 200 ps, and reports this is sufficient due to the reference spur being far beyond the loop bandwidth. It furthermore mentions that the phase noise spectrum is not affected.

This document aims to explore the feasibility of a novel doubling circuit without the use of a delay element and XOR gate. The proposed correction circuit acts as a control loop around the doubler circuit and due to its analog nature is not directly restricted to a maximum resolution. Furthermore it aims to give an more extensive analysis of the performance.

First the PLL feasibility study is given in Chapter 2. The key idea and proposed circuit implementation is discussed in Chapter 3. Chapter 4 focusses on the system analysis of this method where its behavior is quantified from which design rules can be derived. Its noise performance is discussed in Chapter 5, on which Chapter 6 follows with conclusions and recommendations.

Chapter 2

PLL Exploration and Analysis

A Phase Locked Loop (PLL) has several applications, and one of them is frequency multiplication. This Chapter deals with the exploration of a PLL design for frequency doubling, and possibly multiplication by more than 2, to meet the specification as described in Chapter 1. Before doing so, it is instructive to first look at the basic concepts and background of the PLL to further on use it in the exploration and analysis phase.

2.1 PLL Background

The basic concept of a PLL is a feedback system that consists of a Phase Detector (PFD) and a Voltage Controlled Oscillator (VCO)[Fig. 2.1]. Its functionality is based on aligning the phase of the VCO (output) with the phase of the fixed reference frequency (input).

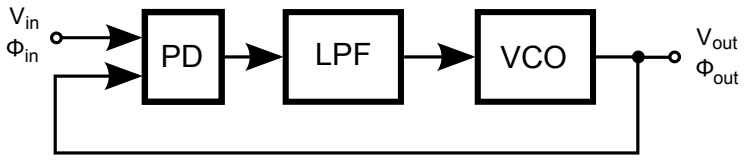


Figure 2.1: Simple PLL system.

The PFD compares the phases of V_{out} and V_{in}, generating an error that varies the VCO frequency until the phases are aligned. The output of the PD, V_{PFD}, consist next to the desired dc component to vary the VCO, of an undesired high-frequency component. This high-frequency component disturbs the control voltage V_{cont} and must therefore be filtered, hence the Low Pass Filter (LPF)[3].

This topology can be modified by adding divider section in its feedback path [Fig. 2.2]. When making use of the previous conclusions one can see for this case that when the phases are aligned the frequencies are equal and hence $f_{out}/N = f_{in}$. This means that the input frequency f_{in} is actually multiplied by a factor N, giving $f_{out} = N f_{in}$.

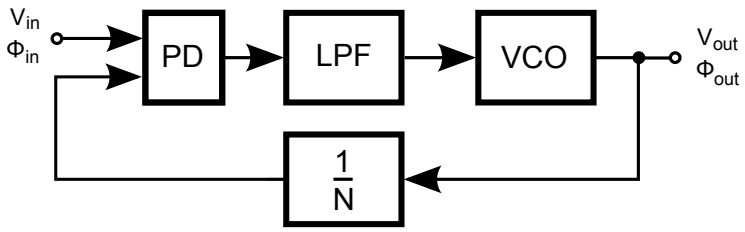


Figure 2.2: PLL with divider in feedback path.

2.1.1 PLL Dynamics

To be able to analyze the behaviour more thoroughly it is important to look at the dynamics of the PLL. This can best be done by s-domain derivations to determine the transfer function $\Phi_{out}(s)/\Phi in(s)$. Where Φ denotes the excess phase. This gives insight in how the output phase tracks the input phase for slow and rapid variations (low and high frequencies). The transfer function of a type I PLL can be derived by constructing a linear model as in Fig. 2.3.

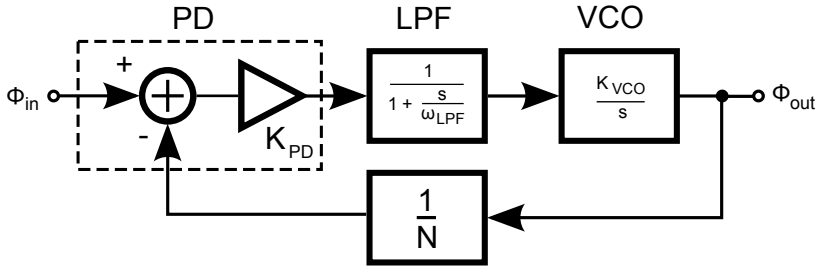


Figure 2.3: Linear model of type I PLL.

When finding the transfer function from input Φ_{in} to Φ_{out} one can write

$$H(s)|_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + \frac{1}{N}K_{PD}K_{VCO}}. \tag{2.1}$$

2.2 PLL Noise Analysis

A noise model of a PLL can be made by using the linear model and include the various noise sources as shown in Fig. 2.4. At first hand, for sake of analysis, only the thermal noise of the noise sources is considered that are normally dominant, where $1/f$ noise is neglected. This leads to the VCO noise having a $1/f^2$ shape due to the integrating action on the white (flat) noise. The spectra of the other noise sources stay white.

To see how the noise, as described above, is transferred in the PLL model, two transfer functions can be formulated. First, the noise transfer function from VCO to PLL output. Second, the noise transfer function from the loop

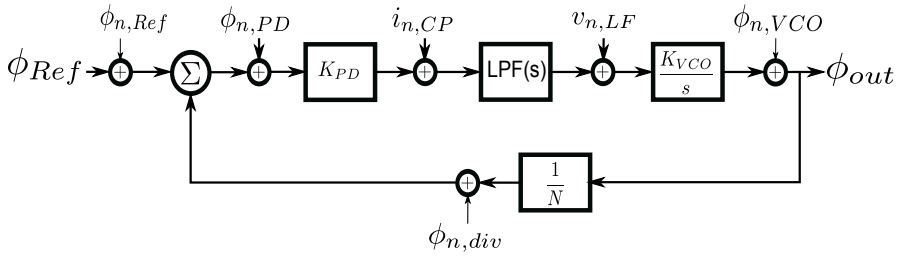


Figure 2.4: Noise model PLL.

components, hence loop phase noise, to the PLL output. The noise transfer function from VCO to PLL output is

$$H_{VCO}(s) = \frac{1}{1 + \frac{1}{N} K_{PD} Z_{LF}(s) \frac{K_{VCO}}{s}}. \tag{2.2}$$

The loop phase noise are the noise contributions when one goes from divider input to PLL output. The noise transfer function from the loop phase noise can therefore be calculated as

$$H_{VCO}(s) = \frac{\frac{1}{N} K_{PD} Z_{LF}(s) \frac{K_{VCO}}{s}}{1 + \frac{1}{N} K_{PD} Z_{LF}(s) \frac{K_{VCO}}{s}}. \tag{2.3}$$

Comparing (2.2) and (2.3) leads to the insight that the VCO phase noise is high pass filtered and the loop phase noise low pass filtered. Fig. 2.5 shows the overall PLL phase noise transfer, where the bandwidth of the PLL is indicated by f_c.

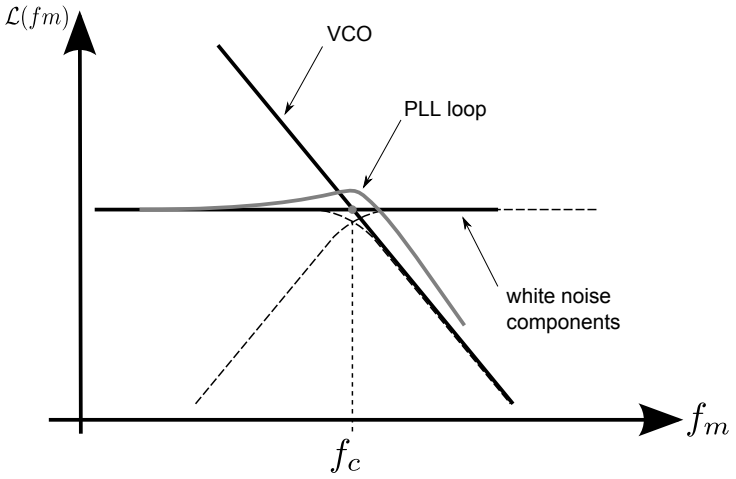


Figure 2.5: PLL output phase noise transfer.

2.2.1 VCO Phase Noise and PLL Benchmarking

In numerous studies [4], [5] it has been found that the phase noise of a VCO is systematically dependent on the important design parameters: oscillation frequency, power dissipation, and offset frequency at which the phase noise is measured. Therefore it is interesting to look at the minimum achievable phase noise produced by a VCO for a given power budget, as has been studied in [6]. For RC relaxation oscillators the minimum achievable phase noise is found to be approximated by [6]

$$PN_{min}(\Delta f) \approx \frac{3.1kT}{P_{min}}\left(\frac{f_o}{\Delta f}\right)^2. \tag{2.4}$$

And for ring oscillators the minimum achievable phase noise is approximated by [6]

$$PN_{min}(\Delta f) \approx \frac{7.33kT}{P_{min}}\left(\frac{f_o}{\Delta f}\right)^2. \tag{2.5}$$

Benchmarking PLL's gives a measure of the quality of PLL designs. The benchmark for PLL's that is recently introduced in [4] is the PLL Figure of Merit (FoM) and gives a measure that is typically determined by the total amount of phase noise and the power that it consumes. The PLL FoM definition as described in [4] is

$$FOM_{PLL} = 10log\left[\left(\frac{\sigma_{t,PLL}}{1s}\right)^2 \frac{P_{PLL}}{1mW}\right]. \tag{2.6}$$

Furthermore in [4] it is derived that if the loop bandwidth is chosen optimally to balance the loopnoise and VCO noise contributions, then:

$$FOM_{PLL} \propto FOM_{loop} + FOM_{VCO}. \tag{2.7}$$

This last statement suggests that the design quality of the PLL loop and the VCO are equally important. conditionally true if the PLL bandwidth is optimized. When going back to Fig. 2.5 one can see that the corner frequency, f_c, is chosen to be there where the $1/f^2$ VCO noise graph intersects with the flat loop noise graph. From [4] it is shown that this is an optimum for a PLL design and is also where the VCO and the loop components contribute equal jitter.

It should be noted that an optimal PLL bandwidth is a theoretical optimum. However, in practice this may not always be possible to achieve because of for example stability criteria. It gives however a good design direction and can provide useful insight for the design of a PLL, as will be discussed in the next section.

2.3 PLL Performance

Now that it is known how PLL noise and performance can be analyzed, it can be used to assess the feasibility of a PLL frequency doubling design with the given specifications as discussed in Paragraph 1.2. With these specifications a FoM can be determined as defined in Paragraph 2.2.1. This gives a rough

indication of the feasibility of a PLL design when compared to known designs in literature [4].

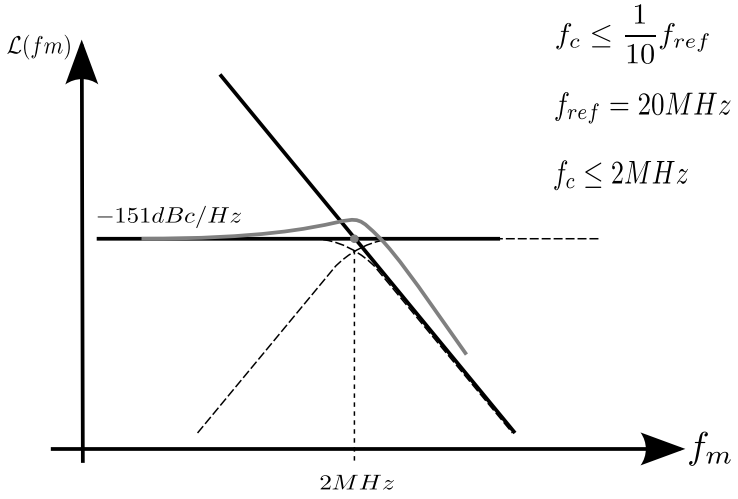


Figure 2.6: PLL output phase noise transfer with specifications.

Fig. 2.6 again shows the transfer graphs of the PLL, now with the specifications. The inset of Fig. 2.6 shows that the stability criteria are met if the PLL corner frequency, f_c, has its maximum at 1/10 of the reference frequency, f_{ref}. Since the specifications dictate that the reference frequency range is 20 - 50 MHz, this leads to a fixed maximum corner frequency, f_c of 2 MHz. The white loop phase noise should have its floor at -151 dBc/Hz, as indicated. When assuming the optimization criteria from Paragraph 2.2.1 it follows that at the corner frequency of 2 MHz, the VCO phase noise should be less than -151 dBc.

To make use of the FoM, it is necessary to express the phase noise specifications in terms of total PLL output jitter. The relation between phase noise and long-term absolute jitter is given as

$$\sigma^2_{t,PLL} = \frac{2\int_0^\infty \mathcal{L}_{PLL}(f_m)\, df_m}{(2\pi f_{out})^2} = \frac{1}{2\pi^2 f^2_{out}} \int_0^\infty \mathcal{L}_{PLL}(f_m)\, df_m. \tag{2.8}$$

Using (2.8) and filling in -151 dBc/Hz for the phase noise, it follows that the total PLL output jitter variance is approximately $2.5 \cdot 10^{-26}$.

Fig. 2.7 shows a graph with low jitter PLL designs from the last decade, for which their FoM's can be determined. The best state-of-the-art FoM's are close to -240 dB. Also, the goal specification is indicated. Note that if a frequency doubling PLL with the given specifications is going to be designed, it would require to have a FoM close to -250 dB, which is 10 dB better than a state-of-the-art PLL.

Next to the given fact that jitter demands seem to be difficult to achieve, it is worthwhile also to have a look at the minimum achievable VCO phase noise. According to the specifications, the power budget should be around 4 mW. When using (2.4) and (2.5) it follows that for -151 dBc/Hz at 2 MHz

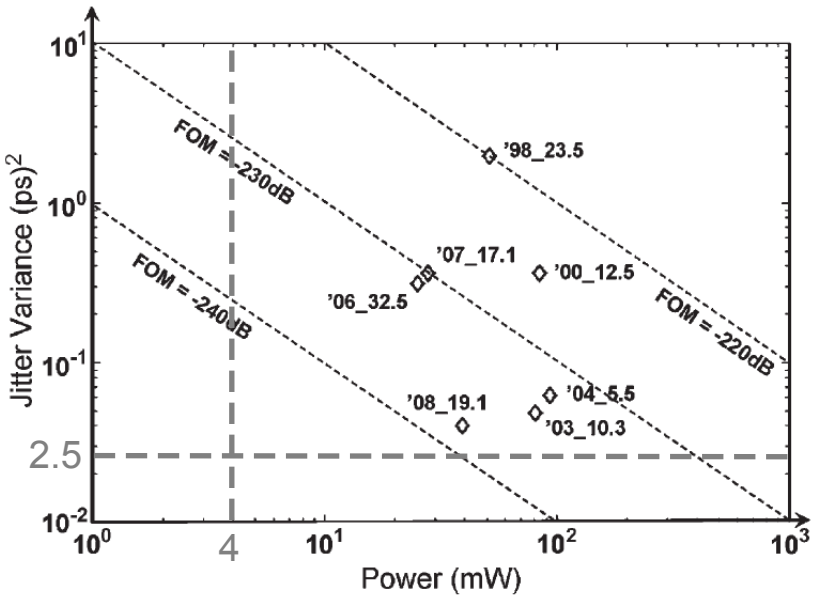


Figure 2.7: ISSCC low-jitter PLL designs with FoM [4].

corner frequency with an oscillation frequency of 100 MHz (worst case), the power that is needed for those phase noise demands is equal to approximately 40 mW (relaxation) and 95 mW (ring).

2.3.1 Specifications Revision

The above section shows that the noise demands put on the PLL design are very stringent. To overcome this, the possibilities are explored to relax the specifications by taking into account a particular synthesizer application, which is a potential application for the doubler. As mentioned before, the frequency doubler then acts as the reference frequency for a frequency synthesizer. This frequency synthesizer is also a PLL design having its own loop bandwidth, and thus also acts as a low-pass filter from phase in to phase out, if its bandwidth is much smaller than the bandwidth of the frequency doubler. The cut-off frequency of this frequency synthesizer is roughly at 200 kHz, and from that point on decays with 20dB/dec. This means for the frequency doubler that from 200 kHz on it is allowed to increase with 20 dbB/dec (see Fig. 2.8). The net result would then give a flat spectrum because the 20dB/dec increase is cancelled by the 20dB/dec decrease of the synthesizer.

As can be seen in Fig. 2.8 this loosens the demands on the VCO by 20 dB, which would therefore drastically reduce the power expenses on that part within an acceptable range. The noise floor within the 200 kHz band however, should still meet the -151 dBc/Hz demands, which is determined by the in-band phase noise of the frequency doubling PLL.

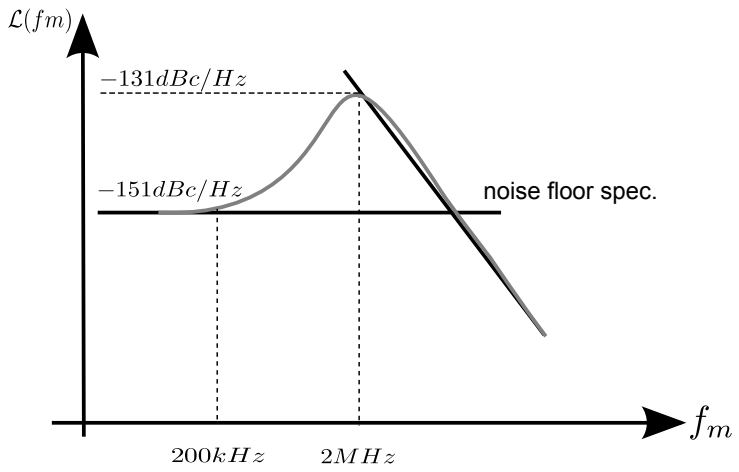


Figure 2.8: PLL output phase noise transfer with revisited specifications.

2.3.2 Fit Specification in State-of-the-Art PLL Design

To get a more realistic insight in how difficult it would be to realize a PLL design with a noise floor of -151 dBc/Hz, state-of-the-art PLL design performance is compared to the given specifications.

The design under investigation is described in [7], and is used because it has the best known in-band phase noise for a given power budget. This PLL's output frequency is 2.2 GHz with a reference frequency of 55.25 MHz, a noise floor of -126 dBc/Hz at 200 kHz offset frequency, and dissipates approximately 7 mW. The aim is to design a frequency doubler with a reference frequency of 20 - 50 MHz, and hence output frequency of 40 - 100 MHz. If [7] is going to be used for this, it can be said that the reference frequencies are roughly the same (assuming the reference frequency of 50 MHz) and the output frequency would undergo a step-down-ratio of $\frac{2GHz}{100MHz} = 20$. With this step-down-ratio the noise floor lowers with 26 dB (20log(20)) and would be at -154 dBc/Hz.

According to the noise analysis in [7], the in-band phase noise is dominated by the crystal output buffer. In [7] an expensive high performance crystal oscillator from Wenzel was used which has an amplitude of $1.8V_{pp}$. The frequency doubler is going to be realized in 65nm technology, which works with a core voltage of 1.2 V. Therefore it would not be possible to get 1.8 V voltage swing, but would practically be at its best $0.9V_{pp}$. Since amplitude lowers the slew rate, which on its turn determines how much stochastic noise is translated to jitter, a lower amplitude has a negative effect on the total in-band noise floor. Therefore, the in-band noise floor increases by 6 dB when halving the reference frequency amplitude. This comes down to a total in-band noise floor of -148 dBc/Hz.

Concluding this shows that a PLL solution would push the boundaries of design. Even this state-of-the-art design would not be able to meet the noise specifications within the given power budget.

2.4 Summary

This Chapter aimed to assess the feasibility of a Phase Locked Loop (PLL) design for frequency doubling, with the given specifications. A Figure-of-Merit (FoM) is used to give a measure of quality for a PLL design. It has been shown that with the given specifications, a PLL design would have such stringent jitter demands that its FoM would require to be almost 10 dB better than state-of-art PLL's. To accompany this, it was also shown that with these demands the minimum power budget that has to be spend on a VCO, greatly surpasses the available power budget. This could partly be overcome by taking in account the loop-bandwidth of the subsequent frequency synthesizer. This however only loosens the VCO demands, where the in-band phase noise of the PLL would still have to meet the same requirements. To assess how stringent this is, a high-end PLL design is examined to see how good this would be under the given specifications. Even with this state-of-the-art design it has been shown that the in-band phase noise is a difficult demand to meet given its power budget.

Chapter 3

Frequency Doubling

Besides realizing frequency doubling by means of Phase-Locked-Loop (PLL), there are alternatives worth exploring. Moreover because a PLL solution does not seem feasible within the given specifications. This Chapter forms the introduction of the exploration to this alternative method.

3.1 Idea

The foregoing Chapter showed that the reference buffer only already accounts for the bigger part of the noise contributions. This leaves little headroom for the rest circuit. Therefore it might be more efficient to only have this buffer in the signal path and find a means of passing through all (both rising and falling) the edges and combining them in such a way that both falling and rising edges become rising edges. This is illustrated in Fig. 3.2.

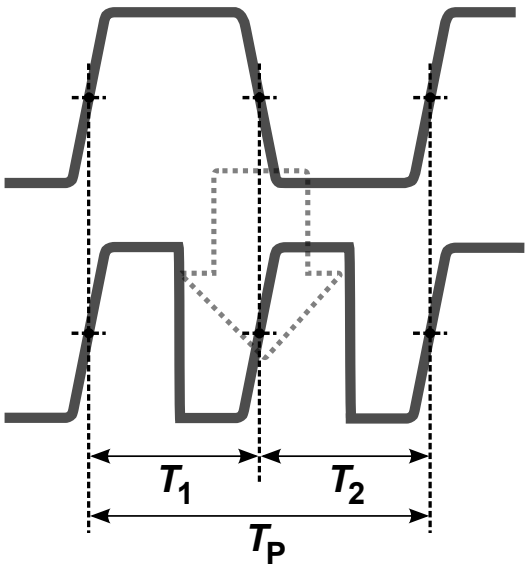


Figure 3.1: Core idea: Use both edges.

The incoming reference frequency, f_{xtal}, is in this case considered to be a trapezium shaped wave, with finite rise and fall times, and having period T_P. It is chosen to consider this shape wave for sake of simplicity, but this can be any type of waveform as long as the edges are well defined. The analysis for any type of waveform is the same. The period time, T_P is considered as being fixed and stable (with the exception of random noise on the edges). Time intervals T_1 and T_2 are ideally half-periods of T_P. In practise these two time intervals depend on the timing of the falling edge in between the two rising edges. By taking advantage of the fact that most clocking circuits are edge sensitive and only "look" at the rising edges, (which makes the falling edges non-critical), it is possible to turn the falling edges of the reference clock into rising edges and combine them with the already present rising edges. This also means that the then present falling edges are non-critical. The created clock signal now has periods equal to half the period of the reference clock, that is T_1 and T_2, hence doubled in frequency.

It is worth mentioning that this has an advantage compared to a PLL solution. It is important to notice that with a PLL the doubled frequency is generated by a relatively noisy VCO, which is than "cleaned up" by the PLL-loop using the crystal rising edges. The Dual-Edge method however has the advantage that it uses the intrinsic clean edges of the reference crystal directly as rising edges for the doubled frequency.

3.1.1 Drawback

Major drawback of this approach is the timing of the falling edge of the reference clock. When this timing is not exactly at half of the period time, T_P, it creates an timing error T1-T2 between adjacent periods of the doubled clock frequency. (Fig. 3.2).

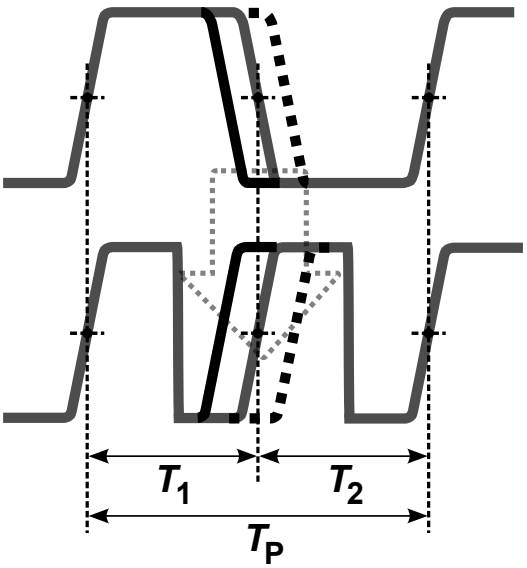


Figure 3.2: Adjacent period error.

As can be seen, the error originates at the reference clock that has unequal half-period times, which is most commonly referred to as duty-cycle error. A duty-cycle of 50% means that the "on" time is 50% of the total period, which makes the adjacent periods equal. A duty-cycle error of 1% means that the duty-cycle is either 49% or 51%, giving unequal adjacent periods. Since the inequality between adjacent periods gives a timing error, it can also be described as a form of jitter. In the following parts of this document the timing error is going to be referred as adjacent period jitter, and is defined as

$$\Delta T = T_1 - T_2 \tag{3.1}$$

The adjacent period jitter that emerges is a recurring phenomenon, that recurs with every period time, T_P, of the reference clock frequency. After all, only the falling edge gives a static timing error, whereas the rising edges relative to each other are fixed with period T_P. This adjacent period jitter can therefore be considered as deterministic jitter. How this error emerges in the frequency domain can be understood by considering the doubled output frequency f_d being modulated by the reference input frequency f_{xtal}. Since it is a deterministic phenomenon it emerges as a spurious tone at the distance of f_{xtal} from the doubled output frequency f_d, in the frequency domain.

3.1.2 Sources of Error

To identify sources of error it is instructive to examine the circuit in Fig. 3.3, a typical crystal oscillator with buffering [8]. The circuit is tuned to the

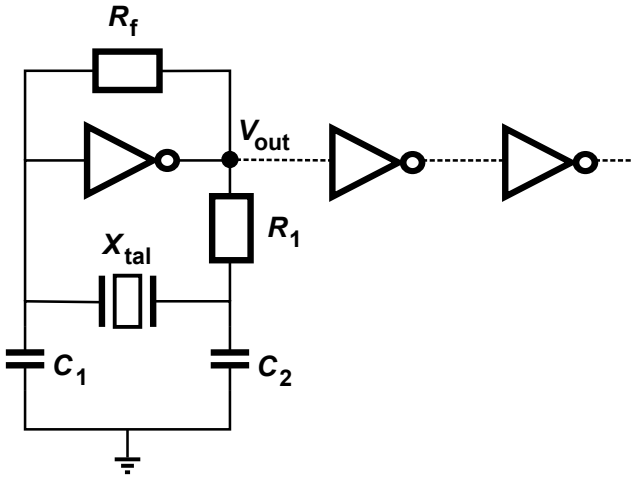
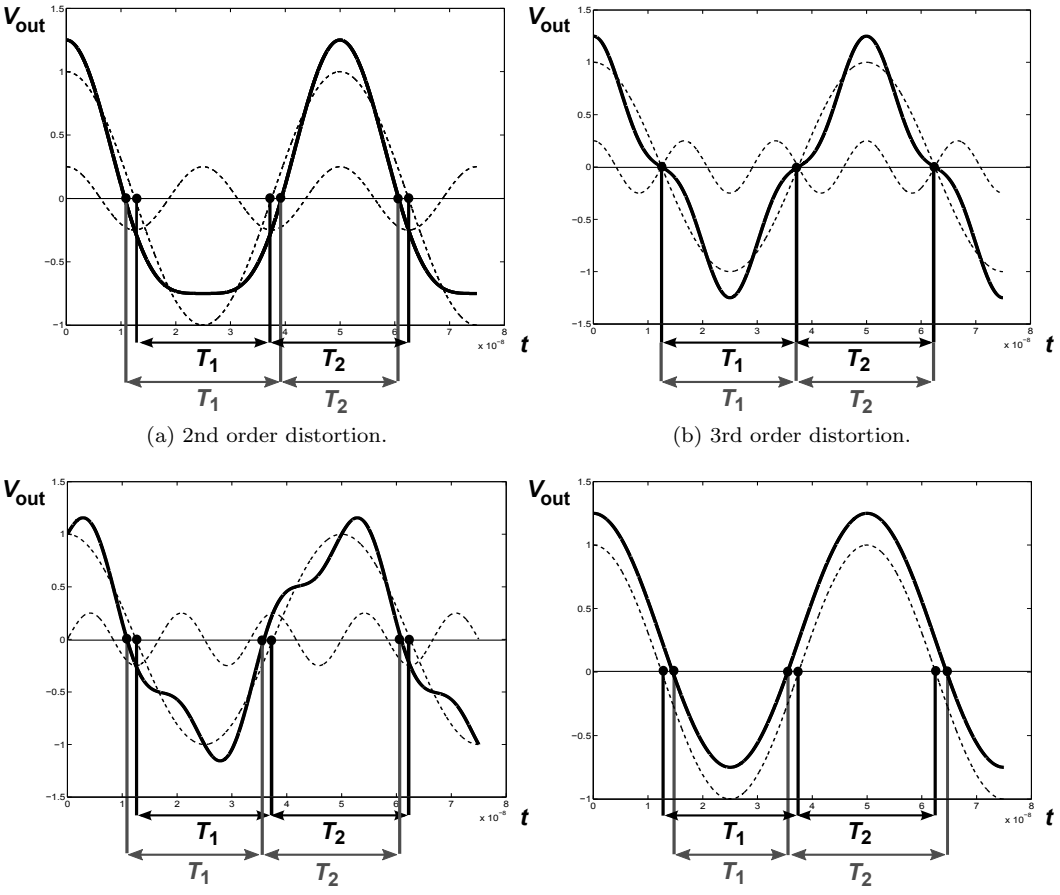


Figure 3.3: A Pierce configuration oscillator circuit.

resonance frequency of the crystal, where ω_0 experiences a total gain of unity and a phase shift of 180°. The eventual oscillator signal that is proposed to be used as the reference frequency of the Dual-Edge Doubler, appears at node V_{out} of the oscillator circuit.

A number a scenarios can be thought of that can introduce time displacements of the zero-crossings of the sine wave at node V_{out}. As shown in Fig. 3.4a the sine wave can have even order distortion. As can be seen even order



(a) 2nd order distortion.

(b) 3rd order distortion.

(c) 3rd order distortion 90 % phase shift.

(d) Offset.

Figure 3.4: Potential sources of adjacent period timing errors.

distortion causes displacements in the zero-crossings such that the adjacent periods T_1 and T_2 are not equal anymore. Odd order distortion on the other hand (Fig. 3.4b and 3.4c)does not introduce adjacent period error. That is, it can give zero-crossing displacements, depending on the phase (Fig. 3.4c), but with equal amounts which leaves T_1 and T_2 equal. The signal can also possess offset, meaning that the dc level can be different than for example an ideal half VDD value. This means that it is not certain on before hand what this level is and has to be anticipated on. Concluding, the sources of error discussed here can all be modelled as adjacent period jitter or duty-cycle error.

3.2 Specifications Revision

The foregoing section showed that a major drawback of the Dual-Edge method is the creation of spurious tones due to deterministic crossing displacements. It would therefore be good to relate the timing error or adjacent period jitter, duty-cycle error, and spurious tone amplitude to each other to be able to

quantify numbers in regard to the specifications.

First it is instructive to relate the commonly used duty-cycle error, DCE, to adjacent period jitter, ΔT, as defined above. The duty-cycle error is simply the deviation from its nominal 50% value. Since adjacent period jitter is defined as the difference between the two half-periods, duty-cycle error in relation to adjacent period jitter can be written down as

$$\Delta T = \frac{2 \cdot DCE}{f_{xtal}} \tag{3.2}$$

Next an expression for the magnitude of the spurious tone has to be found, to be able to directly relate ΔT to the spurious noise demands in the specifications. The spurious tone emerges at a distance of the reference frequency from the carrier. One can see this as the carrier frequency being phase modulated by the reference frequency. Mathematically a phase modulated carrier can be depicted as [9]

$$x_{PM}(t) = A_c cos(\omega_c t + m x_B(t)) \tag{3.3}$$

with m being called the modulation index and

$$x_B(t) = cos(\omega_m t). \tag{3.4}$$

How the phase is modulated is illustrated in Fig. 3.5. The bigger the crossing displacement, the bigger the amplitude of the modulation frequency, and hence the bigger the magnitude of the spurious tone. So to know the spurious tone, one simply has to determine the magnitude of the modulation frequency relative to that of the carrier.

The difference between T_1 and T_2 defines the adjacent period jitter ΔT. This is related to a peak-to-peak phase difference

$$\Delta\phi_{pp} = \Delta T \cdot \pi \cdot f_{out}. \tag{3.5}$$

By assuming that the time displacements at the crossing points are caused by the peaks of the excess phase one can state that the peak phase difference

$$\Delta\phi_p = \frac{\Delta\phi_{pp}}{2}, \tag{3.6}$$

corresponds to two sidebands at $f_{out} \pm f_{ref}$, each with a relative amplitude in relation to its carrier of

$$spur = 20 \cdot log\left(\frac{\Delta\phi_p}{2}\right). \tag{3.7}$$

And hence

$$spur = 20 \cdot log\left(\frac{\Delta T \cdot \pi \cdot f_{out}}{4}\right). \tag{3.8}$$

3.2.1 Redefinition Of Specifications

With the relations between different error definitions determined, it is desirable to have a new look at the system specifications. This is mainly important because of the adjacent period jitter definition and the spur demand in the specifications.

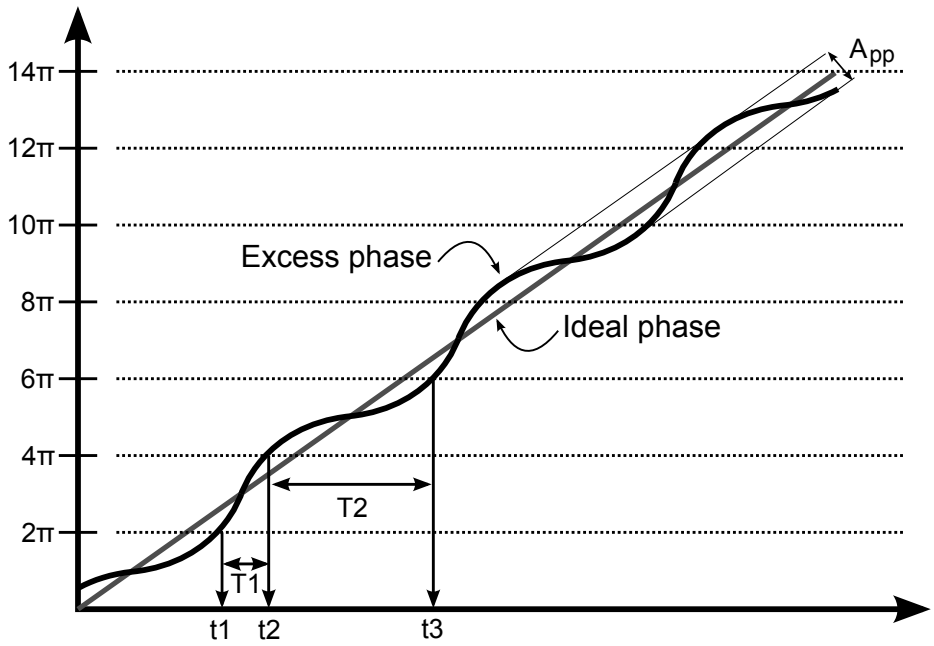


Figure 3.5: Phase modulation.

Output Frequency [MHz]	Spur [dBc]	Adjacent period Jitter [ps]	Duty-Cycle Error [%]
40	-47	140	0.15
60	-33	475	0.7
80	-24	1000	2
100	-16	2000	5

Table 3.1: Spur related to jitter and duty-cycle error.

What not yet is done is to include the transfer from the subsequent stage, the frequency synthesizer. It is already stated that this frequency synthesizer has a loop bandwidth of roughly 200 kHz. This means that the spurious tones would fall outside its bandwidth and significantly suppress them. The transfer reaches a roll-off of eventually 40 dB/dec which indicates that the demands get less stringent for a higher doubler output frequencies. The transfer is given in Fig. 3.6.

From this transfer the suppression can be read for the spread of 20 - 50 MHz doubler input frequency. These will be the offset frequencies for the spurious tones relative to the carrier. It is desired to have the spurious tones suppressed as far as -80 dBc at the synthesizer output. Including the step-up ratios [1], $20 \cdot log\left(\frac{f_{out}}{f_{in}}\right)$, from the doubler output frequency to the frequency synthesizer output frequency. Table 3.1 shows the revised spur, and when using eq. 3.8 and eq. 3.2, adjacent period jitter and duty-cycle-error demands.

[1]Step-up-ratio represents the ratio at which the given noise relative to the carrier will increase/decrease for higher/lower frequencies.

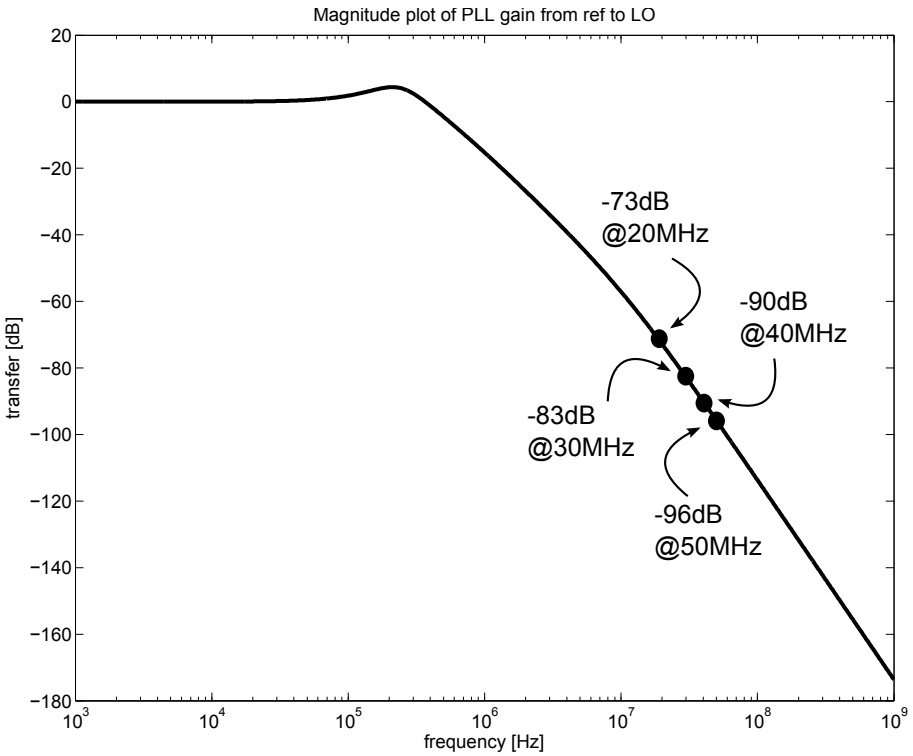


Figure 3.6: Frequency Synthesizer magnitude plot.

3.3 Frequency Doubler Implementation

A means of realizing a Dual-Edge Doubler implementation, as described in the foregoing sections, is to make use of the properties of a differential amplifier. A differential pair typically amplifies the difference between the two input signals, with the properties of having common-mode rejection, high rejection of supply noise, and high output swings (compared to single-ended). The differential signal processing can be exploited when using a differential pair as doubler circuit.

First, a basic differential pair is shown in Fig. 3.7. The symmetric circuit and isolation from ground through a tail current, I_t, makes sure that common-mode levels have minimal influence on the bias currents through the transistors, and have therefore common-mode rejection.

Since its basic functionality is to amplify the difference between two signals, the circuit can also be fed by a sinusoid at one side, and its common-mode level at the other side. When their differential polarity is switched around every time at a non-critical moment between the rising and the falling edges of the sinusoid, one obtains the functionality the rising and falling edges are combined into both rising edges. The functionality is shown in Fig. 3.8a.

When switching the differential polarity at the peak levels of the sinusoid it can be seen (Fig. 3.8b) that every edge has the same polarity at the output of the doubler. This means that the signal is processed as a basic differential pair would, only now the polarity of the input signal is flipped around. By doing so,

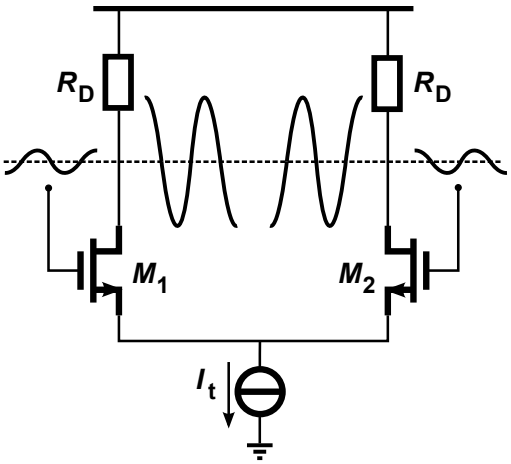


Figure 3.7: Basic differential pair circuit.

the edges relative to each other are flipped, giving every edge the same polarity (since they had opposite polarity).

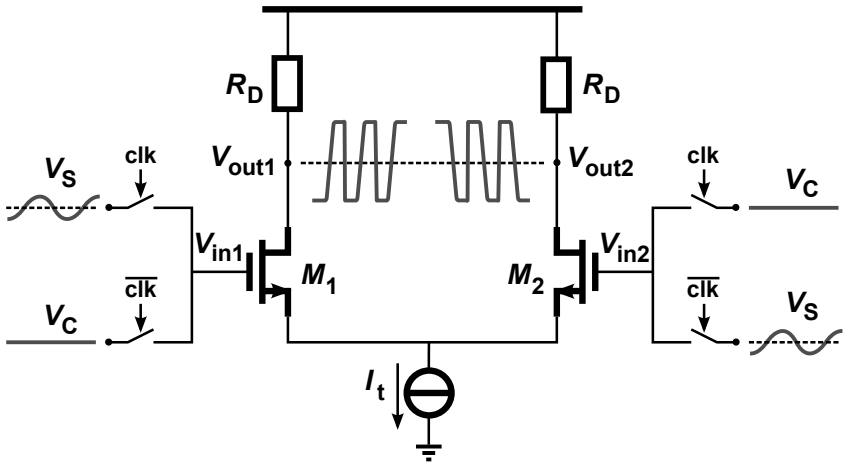
3.3.1 Offset Cancellation

A nice property of this doubler implementation is that the circuit behavior is affected by offsets. Offsets originate from component mismatch in fabrication spreads, by which the symmetry in the circuit is not completely preserved. Components in the left branch, such as resistor, transistor width, or transistor threshold, will not have exactly the same values as the their neighbor components in the right branch. This constitutes a a-symmetry in the circuit, which creates an input-referred offset at the input. What is interesting to look at is the influence of offset on adjacent period jitter in the circuit as shown in Fig. 3.8a. As stated before, the common mode levels of the two input signals have to be such that the zero-crossings of the output signal are equal. This typically means that the common-mode level of the sinusoid and the reference signal have to be equal. Only then, no extra adjacent period jitter is introduced.

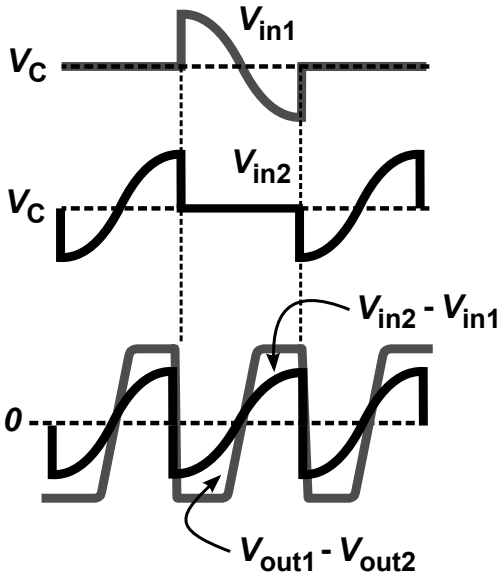
Now consider an offset modelled as an input-referred offset source modelled between the switches and the amplifier input, $V_{OS,in}$, as shown in Fig. 3.9a. The effect that this offset has on the waveforms [2] at the inputs, V_{in1} and V_{in2}, is shown in Fig. 3.9b.

From the waveform it can be seen that the effect of offset on adjacent period jitter actually cancels out. Because polarity of the signal is changed every period, both input signals undergo the same offset voltage, and have opposite effects. A certain offset value now creates a positive time shift on one edge, and the same positive time shift on the next edge as well.

[2]Note that, the effective frequency doubling is actually realized by the switches. The differential pair merely acts as an amplifier for the doubled signal.



(a) Differential pair as doubler circuit.



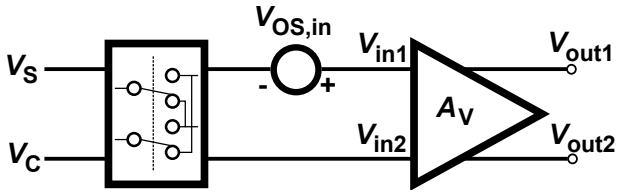
(b) Timing diagram doubler circuit.

Figure 3.8: Differential pair doubler concept.

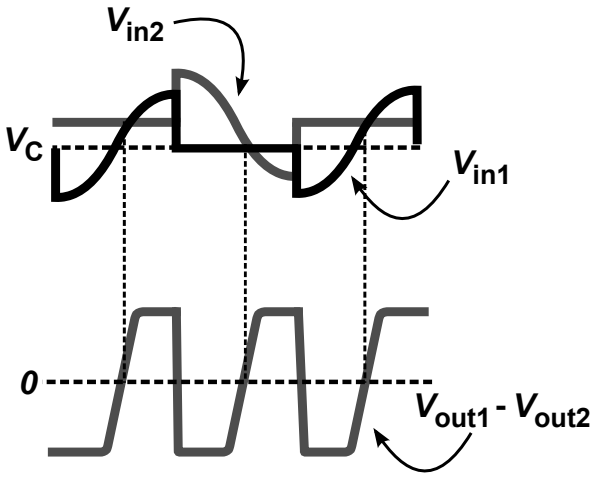
3.4 Error Detection

As discussed before, any circuit that realizes frequency doubling by combining the rising and falling edges of the input reference clock, is sensitive to the timing of these edges. The foregoing section discussed the doubler circuit with sinusoid waveform as input. This can also be another type of waveform, as long as the signal has clear edge transitions. In case of a sinusoid waveform as input, the edge transitions undergo time displacements for even order distortions in the sinusoid (not for odd order distortions). In case of a square waveform, a source of timing errors is duty-cycle error.

The specifications as defined in 3.2.1 Table 3.1 dictate that for a worst case



(a) Block schematic Doubler with offset model.



(b) Offset cancellation timing diagram.

Figure 3.9: Offset cancellation.

situation (doubler output frequency of 40 MHz), the adjacent period jitter should not exceed 140 ps. When the input is a sinusoid waveform, this comes down to approximately 45 dB 2nd order distortion. For a square waveform its duty-cycle error should not exceed 0.15 %. For both input waveforms this is quite demanding, and not realistic to put on typical crystal oscillator circuitry. Therefore there is the need to reduce the error at the output of the doubler circuit by means of a detection and correction circuit.

A means of achieving this is to measure the two time periods, T_1 and T_2, who's difference defines the adjacent period jitter. To be able to make a distinction between the two time periods, the waveform is divided such that time period T_1 represents an 'on' state and time period T_2 represents an 'off' state. The latter functionality can be implemented by means of a divider circuit.

Since the difference between the two time periods is the error of interest, there has to be a way to compare them. This points to the need of a memory element which stores the time information of T_1 and compares it with the time information of T_2. A straightforward approach is to charge a capacitor during time period T_1 and discharge it during time period T_2. This is illustrated in Fig. 3.10.

A circuit that takes care of this operation is shown in Fig. 3.11. This circuit has important features with regard to possible errors that can arise during detection. The operation is done by one current source and one capacitor

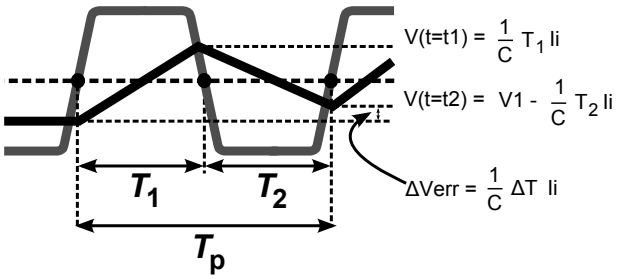


Figure 3.10: Measuring and comparing T_1 and T_2

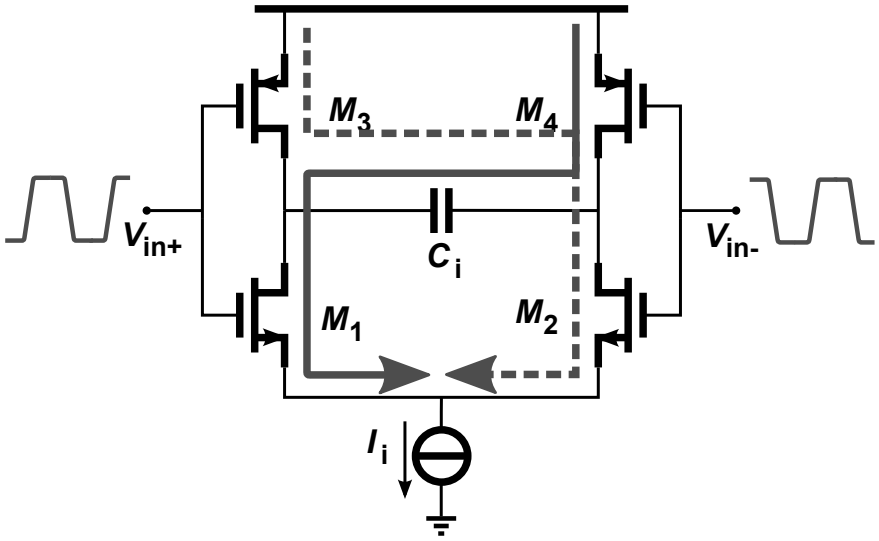


Figure 3.11: Detection circuit

instead of two current sources and/or two capacitors. In this way no mismatch between two of the same components can arise, which minimizes offsets.

The basic operation is to charge and discharge capacitor C_i, during T_1, respectively T_2 (Fig. 3.10). During time period T_1, transistors M_1 and M_4 are turned on, whereas M_2 and M_3 are turned off. This creates a positive voltage across capacitor C_i. During time period T_2 the process is turned around, at which the charge build up is negative. After time period T_2, a rest voltage is present across capacitor C_i representing the time difference between T_1 and T_2.

The above can however also be used as a continues-time switching integrator when using the signal continuously. From simulations it appeared that the circuit in Fig. 3.11 does not act as a pure integrator. Capacitor C_i together with an equivalent ressitance exhibit a time constant $C_i R_{eq}$ (Fig. 3.12). After settling what is left is a differential signal of the square wave having its DC component linear to the average value of the square wave. Hence, the DC component is linear to the adjacent period jitter, ΔT. When making use of Eq. 3.2, the DC relation between ΔV and ΔT can simply be expressed as

$$\Delta V = \Delta T \cdot f_{xtal} \cdot R_{eq} \cdot I_i. \tag{3.9}$$

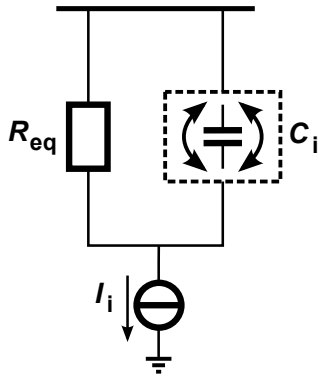


Figure 3.12: equivalent circuit.

And its frequency dependant behavior as

$$\Delta V = \frac{\Delta T \cdot f_{xtal} \cdot R_{eq} \cdot I_i}{sR_{eq}C_i + 1}. \tag{3.10}$$

3.5 Error Correction

Now that the error time signal is detected and available as an error voltage, there has to be a means to use this and correct the input signal. As already briefly mentioned before in the pre-system model there has to be a substraction/addition point somewhere to close the loop. Furthermore, since the output of the detector is a differential signal, there also has to be a way of combining this successfully with the single-ended reference voltage for the doubler [Fig. 3.13].

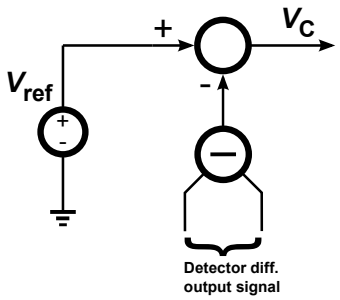


Figure 3.13: Correction model.

This reference voltage for the doubler circuit is chosen to be half V_{DD}, since this is a good approximation of the DC/common-mode level of the reference clock. A switched capacitor circuit that combines the reference voltage out of V_{DD} with the differential output signal of the detector into one single ended signal suitable as corrected reference signal for the doubler circuit is shown in Fig. 3.14. The high glitches from the sampling action can, if necessary, be filtered out by a low-pass filter.

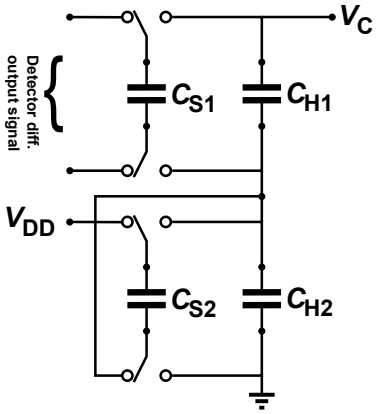


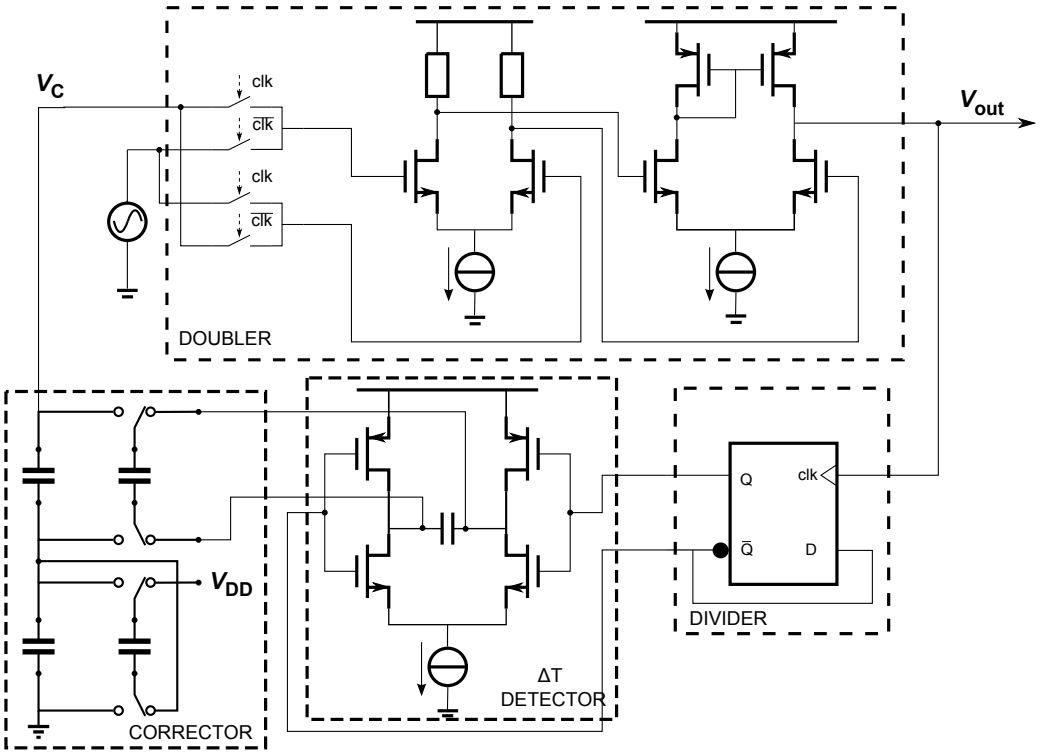
Figure 3.14: Correction circuit.

3.6 Complete Circuit Functionality and Simulations

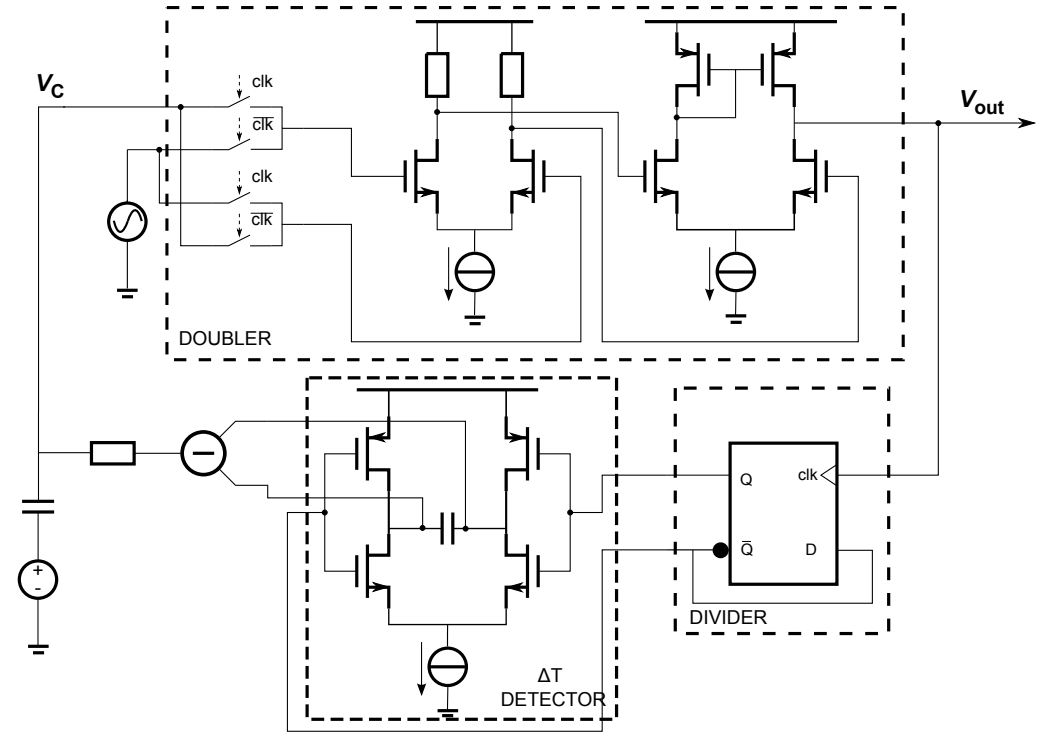
To be able to give a good overview of how the discussed circuit design looks like, the complete circuit schematic is given in Fig. 3.15. As can be seen, all the sub-circuits as discussed in this Chapter are present, which include: doubler, divider, detector, corrector.

The doubler circuit at this point also includes a second stage. This second stage purely amplifies the signal from the first stage, thus making its edges steeper. This can have a positive effect on the noise transfer since steeper edges produce less jitter. Next to that, it also has the functionality to convert the differential signal from the first stage to a single ended signal. This is done because the signal from the second stage has to drive the divider which is implemented as a single ended Flip-Flop.

Fig. 3.16 shows the simulation results of the circuit in Fig. 3.15 for reference frequencies of 20 and 50 MHz. It is chosen give the control voltage response because this also shows the sampled behavior of the correction circuit. The adjacent period jitter response is discussed in more detail in the upcoming Chapter. The results show correct functionality of the circuit in the sense that it brings back the control voltage to half V_{DD}, after a disturbance of 100mV applied at t=3usec.



(a) Time discrete feedback.



(b) Time continues feedback.

Figure 3.15: Complete circuit schematics.

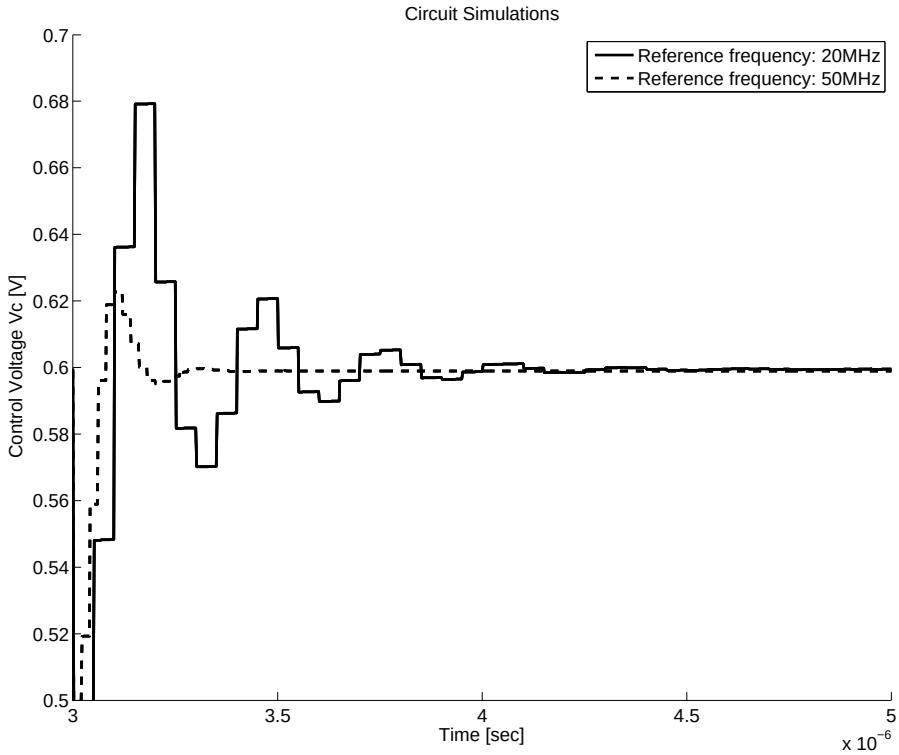


Figure 3.16: Simulation results for input frequencies of 20 and 50 MHz.

3.7 Summary

This Chapter proposed the idea for a new frequency doubling concept, the Dual-Edge Doubler. Differently from a PLL, the Dual-Edge Doubler makes use of both rising and falling edges of the incoming reference frequency and combining them into both rising edges. In this way the reference frequency is doubled. The idea is analyzed and drawbacks with scenarios of possible error sources are sketched. As far as been investigated, all sources of error can be modelled as adjacent period jitter or duty-cycle error. Adjacent period jitter leads to unwanted spurious tones at reference frequency offsets of the carrier. A way of detecting adjacent period jitter is introduced, that gives a correction signal and can be used to adjust and correct the error that has been made. Random noise sources that produce phase noise at the output will be discussed in Chapter 5.

Chapter 4

System Analysis

The foregoing chapter described the electrical circuit and implementations in sub-parts. Now that it is clear how the system on circuit level can be implemented, it would be good to have a detailed system analysis. It is firstly desired to gain insight in how the systems transfer function look like. And secondly to be able to predict the system responses to several parameter values. The analysis is based on the circuit as shown in 3.15b of the previous chapter. A low-pass filter is included in the analysis since this was part of the original circuit design. A low-pass filter is still optional to filter out the high-frequency components from the correction circuit as discussed in Chapter 3.

First, a more detailed system model is given in Fig. 4.1. In this system model every sub-circuit as discussed in the foregoing chapter can be found along with their signals quantities and units.

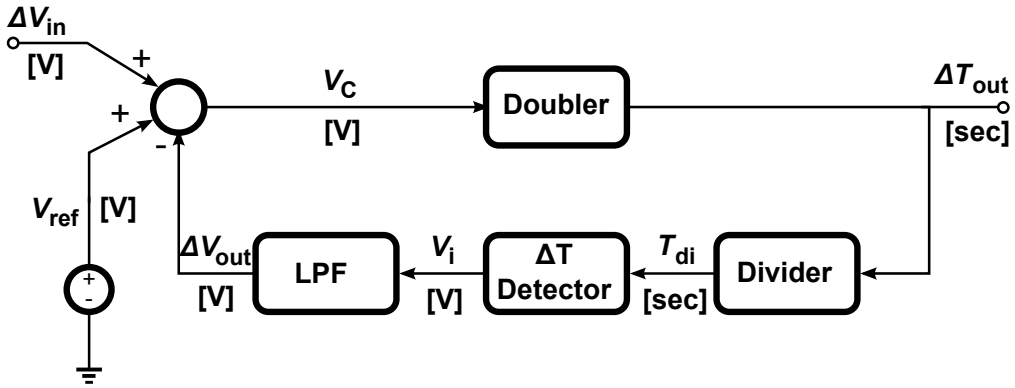


Figure 4.1: Detailed system model.

The input parameter, ΔV_{in}, is the deviation voltage around the reference voltage, V_{ref}, and is not a physical node voltage. Together with the crystal reference frequency it controls the adjacent period jitter, and can thus be seen as the parameter to which the system responds. This makes the crystal reference frequency, in the sense of the control loop, merely an external parameter of the doubler sub-block. This thought can be clarified by considering the timing sketch in Fig. 4.2.

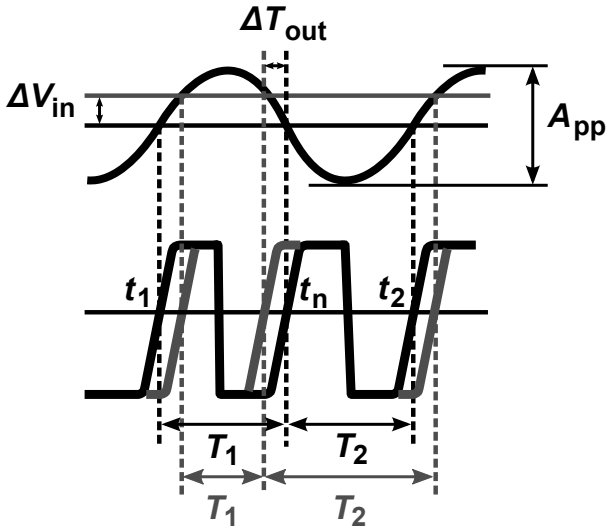


Figure 4.2: relation ΔV_{in} and ΔT_{out}

As indicated before, ideally the reference voltage, V_{ref}, has exactly the same value as the DC voltage level coming from the crystal reference frequency. This gives minimal adjacent period jitter, assuming that the input sine has no 2nd order distortion. One reason to model the problem like this is that the detector circuit detects the timing error and transfers it to a voltage error, hence the feedback signal has the unit voltage and needs to be compared to a signal with the same unit. And secondly, this is a way to define the problem because every form of adjacent period jitter can be related to a voltage difference, ΔV_{in}. The latter relation can be described when considering the zero-crossing timing labels, t_1, t_n (nominal), and t_2, from Fig. 4.2. Then, from definition it is known that

$$\Delta T = T_1 - T_2. \tag{4.1}$$

Where

$$T_2 = t_2 - t_n \tag{4.2}$$

and

$$T_1 = t_n - t_1. \tag{4.3}$$

Substitution gives

$$\Delta T = 2t_n - t_1 - t_2. \tag{4.4}$$

Considering that a voltage deviation, ΔV_{in}, gives a small time deviation, δt on every edge. It can be seen in Fig. 4.2 that this deviation gives a right shift on the first edge, a left shift on the second edge, and again a right shift on the third edge. In algebraic terms:

$$\Delta T = 2(t_n - \delta t) - (t_1 + \delta t) - (t_2 + \delta t). \tag{4.5}$$

$$\Delta T = 2t_n - t_1 - t_2 - 4\delta t). \tag{4.6}$$

This means that the difference between t_1 and t_2 is always the same, namely the period time. Therefore, the adjacent period jitter ΔT is a measure that shifts within the fixed time frame of the period time.

$$\Delta T = 4\delta t. \tag{4.7}$$

Where

$$\delta t = \frac{\Delta V_{in}}{SlewRate}. \tag{4.8}$$

And so

$$\Delta T = \frac{4\Delta V_{in}}{SlewRate}. \tag{4.9}$$

4.1 Linearized System Model

In order to quantify the behavior of this circuit design's system model, it is essential to approximate a linearized model of the system. To do so, the system can be linearized around the nominal time T_N, which is essentially shown in the derivations as shown in the last section.Since adjacent period jitter is the measure of interest every sub-circuit can be considered as linearized within this deviation regime. When following this, the system model from Fig. 4.1 can be re-stated as shown in Fig. 4.3. For sake of completeness it is chosen to have as

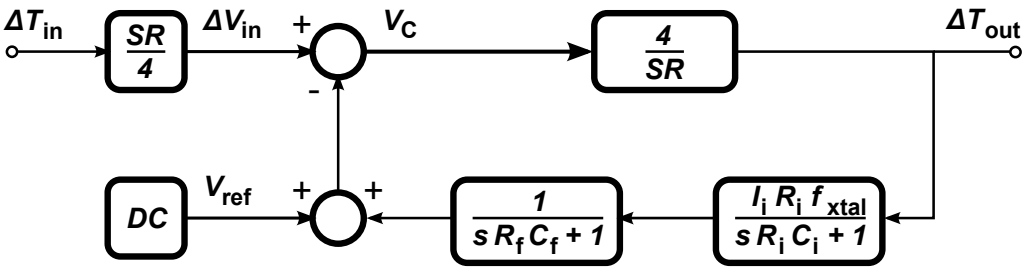


Figure 4.3: Linearized system model.

input quantity ΔT_{in} which coincides with ΔT_{out} as an output quantity. This gives a better overview, since a certain ΔT_{in} at the input has to be reduced to a minimum value for ΔT_{out} at the output, although the essential control loop is from ΔV_{in} to ΔV_{out}.

The transfer of the doubler sub-circuit is merely the relation from Eq. 4.9. Again it is important to state that the actual doubling work is done by the flipping actions as carried out by the switches, where the amplifier merely amplifies the signal after it is doubled. This means that the slew rate of the incoming crystal signal is the parameter in the transfer. Another important aspect is that an ideal divider is transparent to every rising edge that it is being fed. Essentially a divider toggles at every rising edge. Therefore the divider can be seen as a sub-circuit that merely makes a waveform translation, suitable for the detector to work with, and can be left out of the equations[1]. The detector itself has the transfer function which has been described by Eq.

[1] As already stated this counts for an ideal situation. In practise the divider has influence for its finite rise and fall times.

3.10 in Chapter 3. This together with the transfer function of the low pass filter makes a loop transfer of the 2nd order, whereas the open loop transfer is expressed as

$$H(s)|_{open} = \frac{\Delta V_{out}}{\Delta V_{in}}(s)|open \tag{4.10}$$

$$H(s)|_{open} = \frac{4}{SR} \cdot \frac{I_i R_i f_{xtal}}{sR_iC_i + 1} \cdot \frac{1}{sR_fC_f + 1}. \tag{4.11}$$

Or in a different form

$$H(s)|_{open} = \frac{4}{SR} \cdot \frac{I_i f_{xtal}}{sC_i + \frac{1}{R_i}} \cdot \frac{1}{\frac{s}{\omega_{LPF}} + 1}, \tag{4.12}$$

which shows that the pole due to the low pass filter is fixed. The second pole introduced in the detector's integrator is more or less a dynamic parameter because of its dependence on the equivalent resistance in the circuit. This also reveals that the open loop gain will not go to infinity for frequencies approaching zero, which indicates that the closed loop step response will exhibit a steady-state error. The closed loop has a unity feedback which makes its transfer

$$H(s)|_{closed} = \frac{\frac{4}{SR} I_i f_{xtal}}{(\frac{s}{\omega_{LPF}} + 1)(sC_i + \frac{1}{R_i}) + \frac{4}{SR} I_i f_{tal}}. \tag{4.13}$$

4.1.1 Behavioral quantification

Eq. 4.13 suggests due to its second-order transfer function, that the step response of the system can be overdamped, critically damped, or underdamped. It would be helpful in designing the system to be able to derive conditions for these cases. To do so, it is convenient to rewrite in a more familiar form as used in control theory,

$$H(s)|_{closed} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{4.14}$$

with ω_n and ζ being the systems resonance frequency and damping factor respectively.

Rewriting Eq. 4.13 in the form of Eq. 4.14 gives

$$H(s)|_{closed} = \frac{\frac{\frac{4}{SR} I_i f_{tal}}{R_f C_f C_i}}{s^2 + s(\frac{1}{R_iC_i} + \frac{1}{R_fC_f}) + \frac{1}{R_iC_iR_fC_f} + \frac{\frac{4}{SR} I_i f_{tal}}{R_fC_fC_i}}. \tag{4.15}$$

Comparing this to the standard form leads to a relation for the system's resonance frequency,

$$\omega_n = \sqrt{\frac{1}{R_iC_iR_fC_f} + \frac{\frac{4}{SR} I_i f_{tal}}{R_fC_fC_i}}, \tag{4.16}$$

and for the system's damping frequency,

$$\zeta = \frac{\frac{1}{R_iC_i} + \frac{1}{R_fC_f}}{2\sqrt{\frac{1}{R_iC_iR_fC_f} + \frac{\frac{4}{SR} I_i f_{tal}}{R_fC_fC_i}}}. \tag{4.17}$$

As mentioned before the system exhibits a steady-state error due to impurity of the detector's integrator circuit. An important issue because this error is not allowed to exceed the minimum allowable error as stated in the specifications section. It is relevant to also be able to quantify this error seen its importance.

Before any approximation can be made, it is important to first derive a basic expression for the error signal for system in Fig. 4.3. Again, because of unity feedback, the error is

$$V_C = \Delta V_{in} - \Delta V_{out} = \Delta V_{in} - H(s)|_{open} V_C \tag{4.18}$$

which can be expressed in terms of V_C only as

$$V_C = \frac{\Delta V_{in}}{1 + H(s)|_{open}}. \tag{4.19}$$

Now the steady-state error can be approximated by making use the final-value theorem

$$\lim_{t\to\infty} v_c(t) = \lim_{s\to 0y} sV_C(s) \tag{4.20}$$

$$\lim_{t\to\infty} v_c(t) = \lim_{s\to 0} \frac{s\Delta V_{in}(s)}{1 + H(s)|_{open}}. \tag{4.21}$$

Where ΔV_{in} is a unit step input, and so

$$\Delta V_{in}(s) = \frac{1}{s}. \tag{4.22}$$

The steady-state error of the closed-loop system then becomes

$$e_{ss}(t) = \lim_{s\to 0} \frac{1}{1 + H(s)|_{open}}. \tag{4.23}$$

4.1.2 Time Discrete Feedback

The circuit as described in Fig. 3.15a of Chapter 4 has a different transfer model as the system that has been described until now which is based on the circuit in Fig. 3.15b of Chapter 4. The correction circuit in Fig. 3.15a makes use of sample-and-hold which involves a dead-time. Fig. 4.4 shows the system model, where the LPF is replaced by the dead-time transfer.

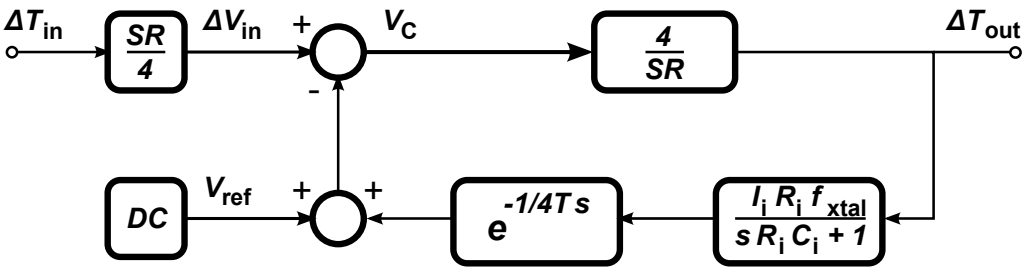


Figure 4.4: Linearized system model with discrete feedback.

The open-loop transfer is

$$H(s)|_{open} = \frac{4}{SR} \cdot \frac{I_i R_i f_{xtal}}{sR_iC_i + 1} \cdot e^{-\frac{1}{4}Ts}. \tag{4.24}$$

The closed loop transfer function can best be written in the Z-domain to be able to approximate the dead-time. This is done by using the forward-euler approximation which can be solved using Matlab. This is nothing more than a transformation of the transfer model as described in the foregoing section.

4.2 Simulation comparison

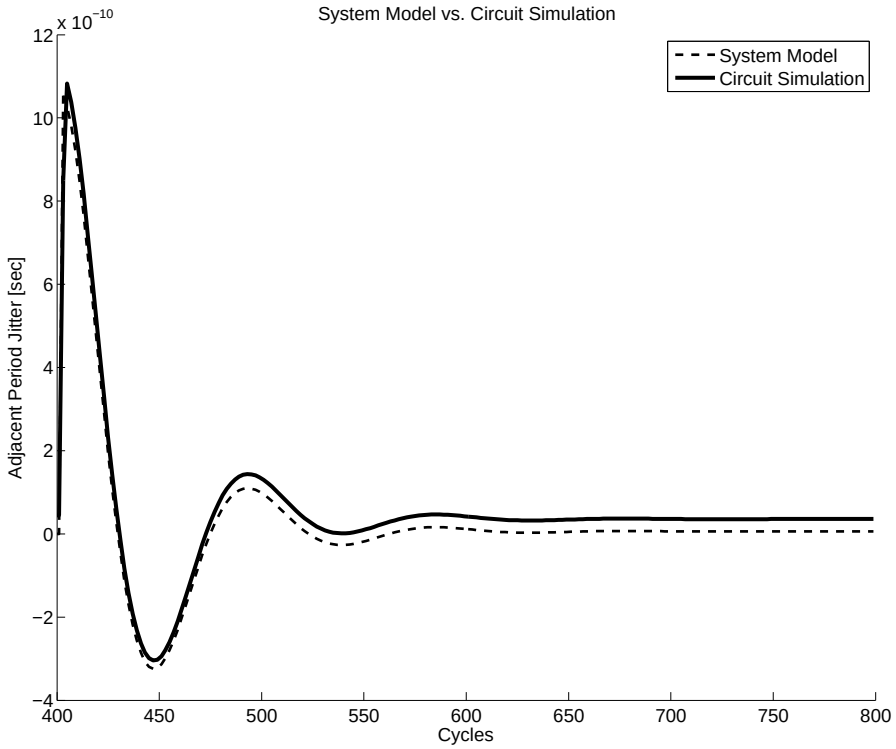
The system analysis along with its behaviorial quantification allows to design the circuit such that it behaves according to things such as settling time, overshoot and steady-state error. The model as described predicts the circuits behavior, so it is a first necessity to examine if the predictions of the system model match circuit simulations.

4.2.1 Time Continuous Model

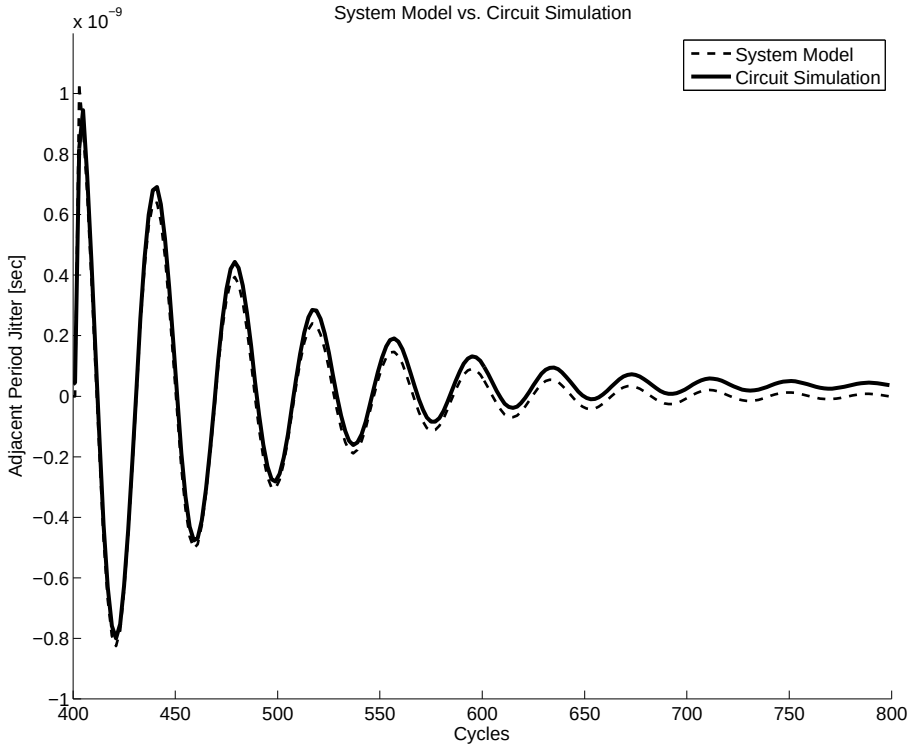
Fig. 4.7 shows two step response plots in which the system model predictions are compared with the circuit simulations[2] based on the circuit in Fig. 3.15b of Chapter 4. For the step response in Fig. 4.5a an input frequency of $20M$Hz is used with the following circuit component values: $I_i = 100\mu$A, $C_i = 50p$F, $R_f = 100k$ohm, and $C_f = 5p$F. For these values the step response of the approximated system model that predicts a resonance frequency ω_n of approximately $2.9E6$rad/sec and a damping of approximately 0.34. The same goes for Fig. 4.5b, where the circuit component values are: $I_i = 100\mu$A, $C_i = 5p$F, $R_f = 100k$ohm, and $C_f = 10p$F. This gives a resonance frequency ω_n of approximately $6.3E6$rad/sec and a damping of approximately 0.08. Both simulations show good accordance with predictions of the system model, apart from a small static offset error in the circuit simulations. The latter can be subscribed to small offsets in the detector circuit that occur when the driven signal has unequal rise and fall times. The error however is in the range of 50 ps, which is still far beyond the minimum specification of 140 ps for this input frequency.

For the simulation results as shown in Fig. 4.7 the value of R_i that is the equivalent resistance in the detector circuit, could be still neglected. This can also be understood from Eq. 4.17, that shows that if the part $1/R_iC_i$ is relatively small compared to $1/R_fC_f$, R_i does not play a significant role in the damping of the system. This changes however for different circuit component values and different W/L values for the transistors in the detector circuit. The simulation results that are shown in Fig. 4.6 give two different circuit simulations with their system model predictions. For both simulations the component values are: $I_i = 10\mu$A, $C_i = 1p$F, $R_f = 100k$ohm, and $C_f = 50p$F. One simulation is carried out with a W/L of the transistors of 1.6 and gives a fairly small damping ratio of 0.05. For this case R_i is not accounted for in the system model and gives a reasonable prediction. For the other simulation

[2]Note that the horizontal axis of the plots are in units of cycles. One cycle equals the period time of the output frequency.



(a) Resonance frequency and damping of approximately $460kHz$ and 0.34 respectively.



(b) Resonance frequency and damping of approximately $1MHz$ and 0.08 respectively.

Figure 4.5: Step responses of system model vs. circuit simulations for different design parameters.

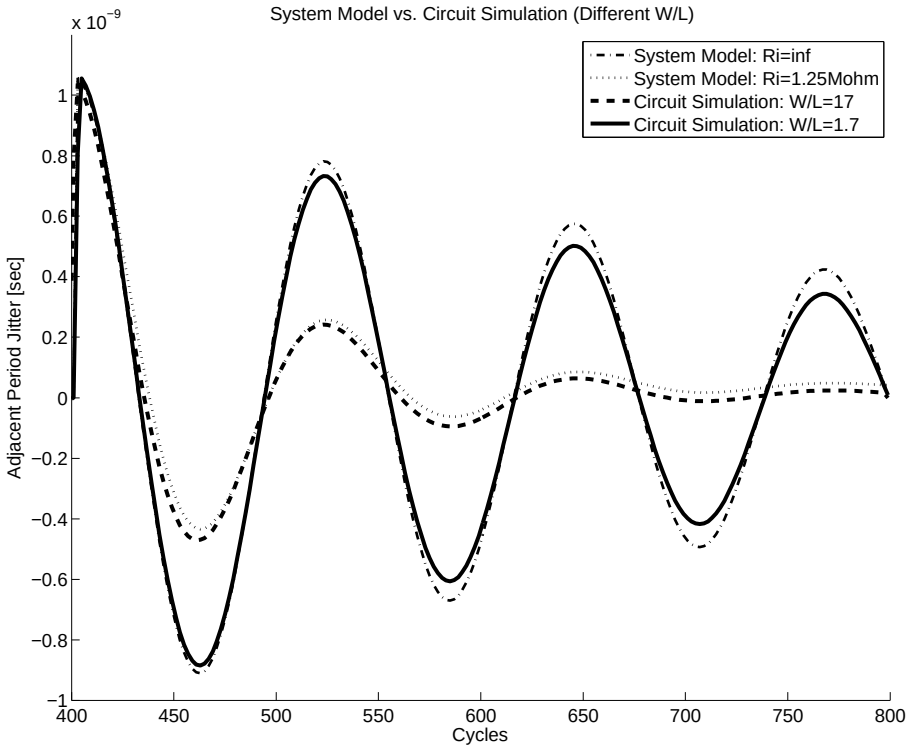
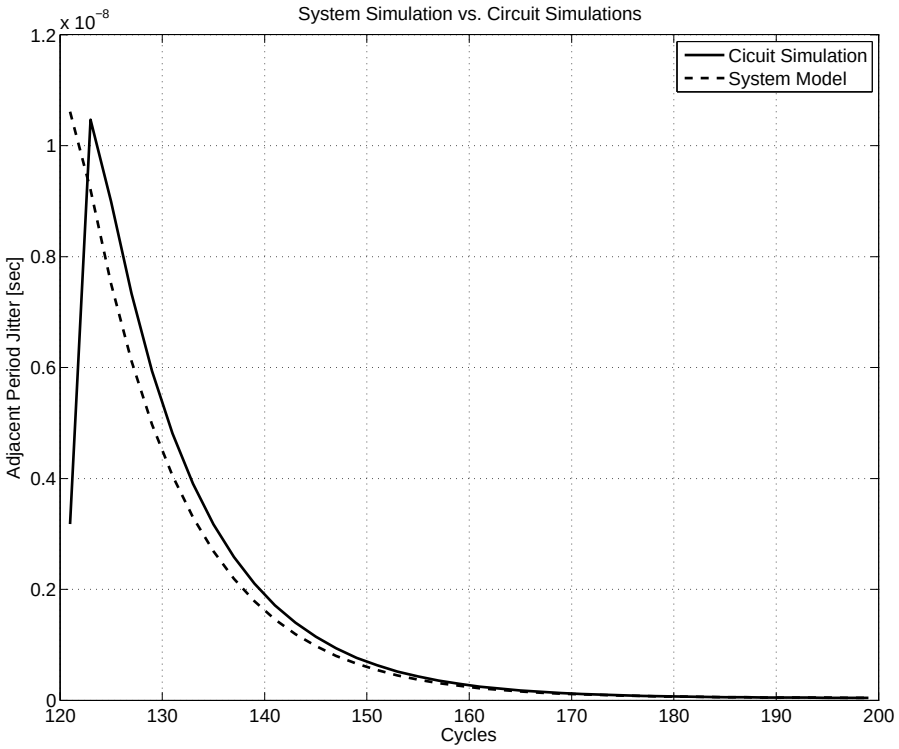


Figure 4.6: Simulation results for different W/L values.

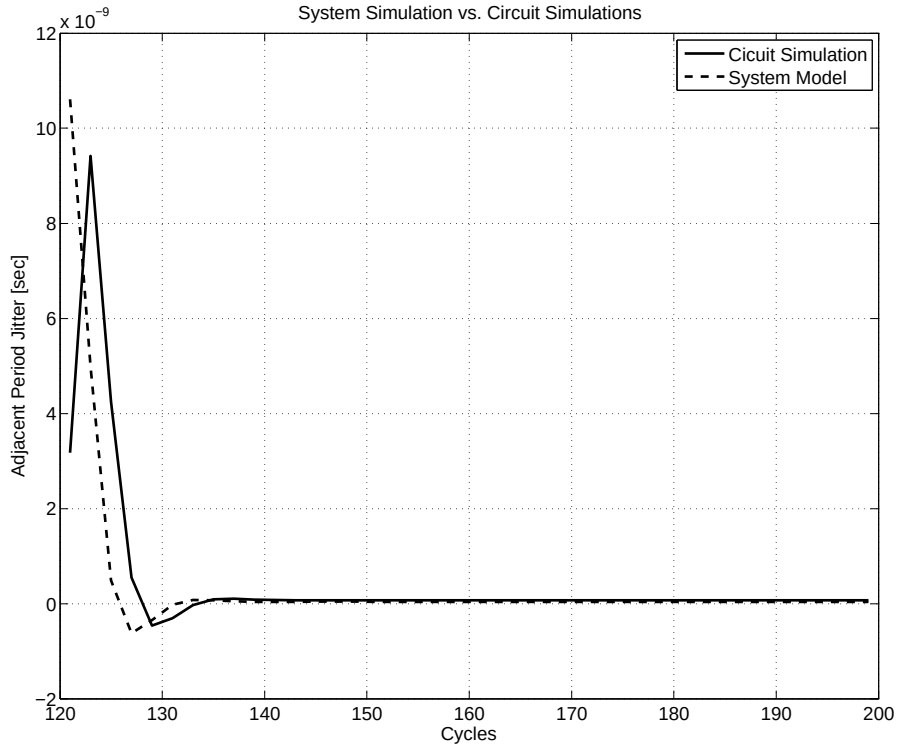
a W/L of 16 is taken which shows a significant change in damping ratio. Now R_i has to be taken in account for the system model to match up, which then gives a damping of 0.24. These results indicate that for higher W/L ratios, the off-resistances cannot be neglected and have to be taken in account to make an accurate prediction.

4.2.2 Time Discrete Model

The following simulation results are based on the circuit as shown in Fig. 3.15a of Chapter 4. Fig. 4.7a shows the step response with circuit component values: $I_i = 100u$A, $C_i = 50p$F, C_h of the first track-and-hold circuit is $10p$F and of the second track-and-hold is $1p$F. The same goes for Fig. 4.7b with circuit components values: $I_i = 100u$A, $C_i = 5p$F, C_h of the first track-and-hold circuit is $10p$F and of the second track-and-hold is $1p$F.



(a)



(b)

Figure 4.7: Step responses of system model vs. circuit simulations for time-discrete model.

4.3 Summary

This chapter described a detailed system analysis of the circuit design as discussed in Chapter 3. Its behavior is quantified and the predictions are compared to circuit simulations that show good agreement to each other. With the behavior correctly quantified it is possible to further optimize and/or extend the circuit design. It allows insight in system trade-offs which will become important when analyzing the system's noise behavior as will be done in the next Chapter.

Chapter 5

Noise Estimation

One of the motivations to choose for the side-track of the Dual-Edge approach was that a PLL solution showed difficulties in meeting the phase noise demands. This Chapter will estimate the noise performance of the Dual-Edge Doubler by identifying and quantifying noise contributions. This will be supported with simulation results. Before doing so, a short introduction in the theory behind the noise estimation for circuits with a sampled nature will follow. The 'SpectreRF' documentation is not always very clear about the mathematical definition of the output quantities produced by PSS analysis. The most useful information that can be found mainly comes from the website designerguide.com [10], [11], [12].

5.1 Noise in Sampled Systems

The doubled frequency as generated by the proposed Dual-Edge method is used as an edge-sensitive clock for the next stage. The next stage is triggered by the rising edge, which is also the reason why only this edge deserves further attention. More specifically it can be considered that the next stage is triggered by the output rising edge of the Doubler when it crosses a certain threshold value V_{th}. For CMOS gates this is usually around half the supply voltage. This is illustrated in Fig. 5.1.

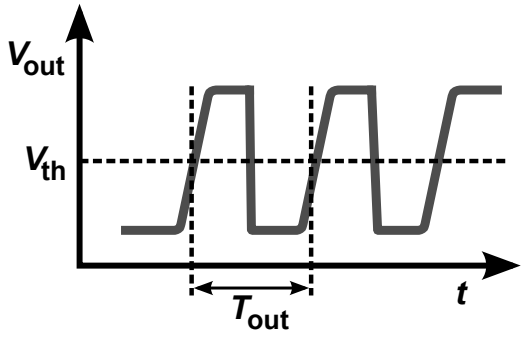


Figure 5.1: Waveform of Doubler output.

5.1.1 Cyclostationary Noise

It may be clear that the noise of interest is the noise that is present on the rising edge, and more specifically at threshold moment V_{th}. Because of the noise present at this threshold moment, it triggers the next stage at some time instant different from the ideal. To understand the noise behaviour, the notion of cyclostationary noise is useful.

The name cyclostationary noise refers to the fact that it is cyclic or periodic stationary[1] noise. It is generated by circuits whose operating points change periodically in time. The time-varying operating point modulates the output noise of noise sources whose output noise depends on a operating point (one can think of it as a voltage controlled noise source). Cysclostationary noise occurs in every non-linear circuit that is driven by a large periodic signal, which are for example inverters, dividers, and the Dual-Edge circuit as proposed in this Thesis. To clarify the above, the cyclostationary nature of the noise at the the output of the Doubler is illustrated in Fig. 5.2.

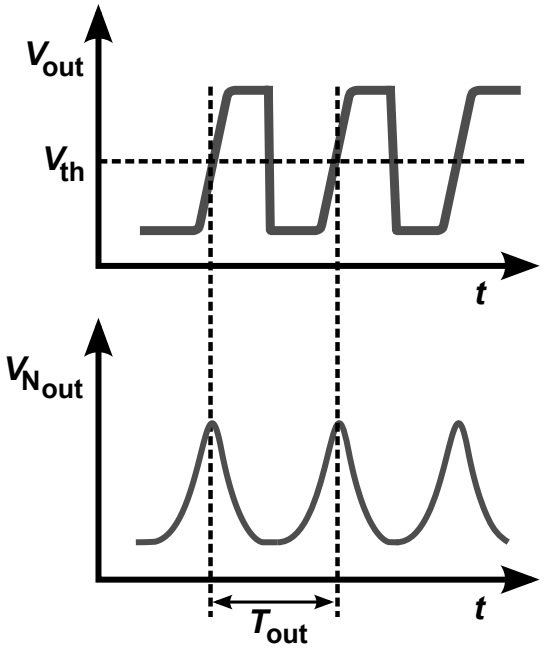


Figure 5.2: Illustration of cyclostationary noise at output of Dual-Edge Doubler circuit.

5.1.2 Noise Sampling

To be able to see the cyclostationary noise, one has to obtain a instantaneous Power Spectral Density (PSD)[2]. An instantaneous PSD is taken by sampling

[1] Stationary noise is noise whose static properties do not change over time.

[2] The traditional PSD is referred to as the time-averaged PSD, what is measured by a traditional spectrum analyzer when the frequency of cyclostationarity is well beyond the bandwidth of the analyzer. In this way the cyclostationary nature cannot be tracked and will thus be averaged out.

the noise at the desired threshold moment with the same periodicity as the cyclostationary noise [Fig. 5.3]. This results in a time-discrete noise samples for which the PSD can then be computed. This can be produced by 'SpectreRF' by using the strobed pnoise function.

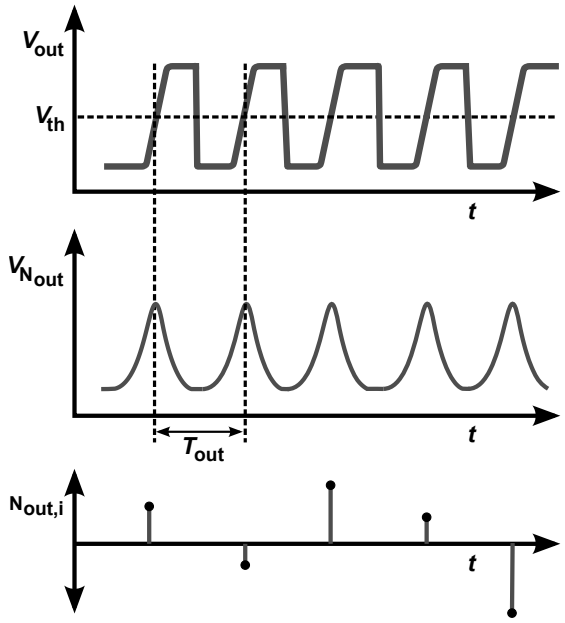


Figure 5.3: Sampling of noise at threshold moments (lower graph is magnified).

Since the stationary noise is modulated by a periodic signal, the noise will manifest itself around the fundamental of the periodic signal and the harmonics it produces. This together with the sampled nature of the noise process makes that all the noise contributions fold back into one band whose spectrum is periodic in f_s (which is equal to the modulation frequency). This is clarified in the illustration of Fig.5.4.

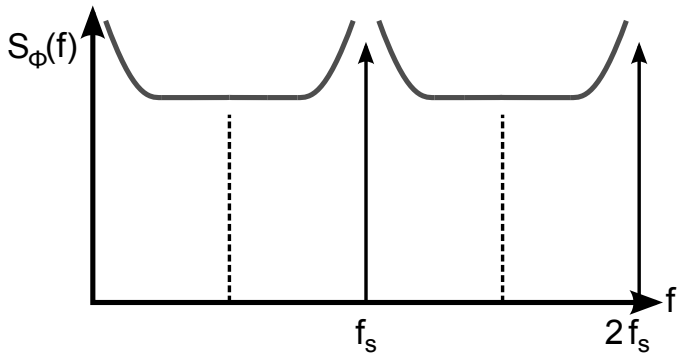


Figure 5.4: Folding of the noise spectrum.

Correct simulations using the above described method means that enough sidebands have to be included into the simulation to take account of all the

noise folding components. How many sidebands this should be depends on the effective bandwidth of the circuit.

5.2 Noise and Jitter

In clock circuits it is more desirable to express noise in terms of jitter. Jitter is the time domain equivalent of phase noise in the frequency domain. The directly observed noise on an edge at a certain crossing moment V_{th} causes a time displacement of the crossing moment (jitter) whose magnitude depends on the steepness of the edge. Therefore, noise in the voltage domain is related to jitter in the time domain by the time derivative of the edge or slew rate (SR)[Fig. 5.5]. This means that a steeper edge converts less noise from the

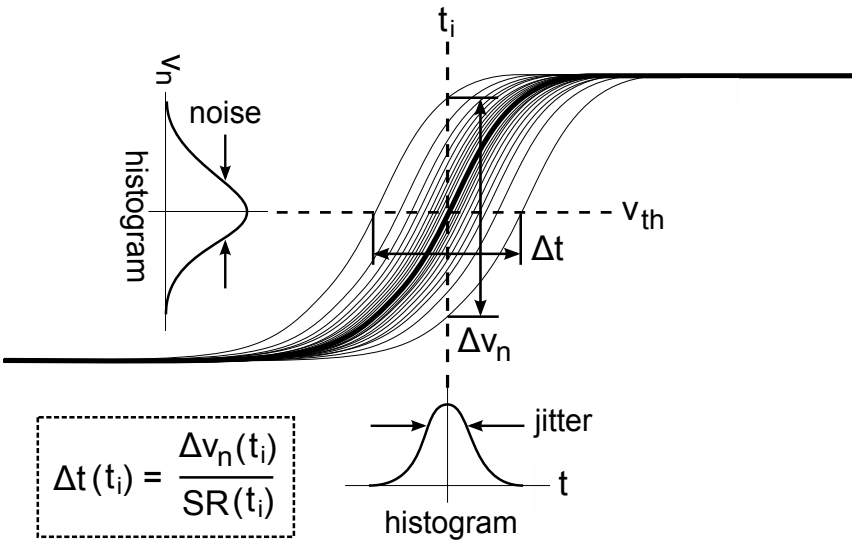


Figure 5.5: Relation of noise in the voltage and jitter in the time domain.

voltage domain to jitter in the time domain.

5.2.1 Definitions

There are different kinds of definitions of how to describe and quantify noise. This subsection is meant to define what kind of relations and definitions the author of this Thesis uses to estimate the noise in the next sections.

The most common measure is the power spectral density of the voltage, S_v. This is what is usually directly observed by a spectrum analyzer and the most common measure in simulators such as 'SpectreRF'[3]. When talking in terms of phase noise, S_ϕ is used, which is the power spectral density of the phase.

[3]This is because traditional noise analysis in circuit simulators derived from SPICE is AC noise analysis, where the noise voltage versus frequency is analyzed for a circuit which is linearized around its (static) bias point. 'SpectreRF' extends this capability to circuit with time varying bias point ('pnoise').

A third measure is $\mathcal{L}$, which is the power spectral density of the voltage, S_v, normalized to its carrier.

To relate this to the sampled cyclostationary noise of interest, SpectreRF produces $S_{v_i}(f)$. This is the spectral density of the random time-discrete noise using the process as described in Paragraph 5.1. According to [12] this is related the the spectral density of the phase by

$$\mathcal{L}(f) = 2 \cdot \left(\frac{\pi f_{out}}{SR} \right)^2 \cdot S_{v_i}(f). \tag{5.1}$$

To the best of the authors knowledge, the spectral density definitions as used by SpectreRF are single-sided representations.

For jitter, the definition absolute jitter[4] is used. The variance of absolute jitter is related to the total area of the power spectrum of the phase[5][13]

$$\sigma_A^2 = \frac{1}{2(\pi f_{out})^2} \int_0^{f_{out}} \mathcal{L}(f)\, df. \tag{5.2}$$

Now it is possible to calculate the jitter from the spectral density $S_{v_i}(f)$ that SpectreRF produces, by combining 5.1 and 5.2, which yields

$$\sigma_A^2 = \frac{1}{SR^2} \int_0^{f_{out}} \mathcal{L}(f)\, df. \tag{5.3}$$

5.3 Noise Estimation and Simulations

To come to a noise estimation, first the most dominant noise sources have to be identified. Fig. 5.6 shows the Dual-Edge Doubler system model including the control loop as discussed in Chapter 4. As indicated, the dominant noise sources to be expected are the amplifier after the doubling switches, the sample and hold circuit and the ΔT Detector.

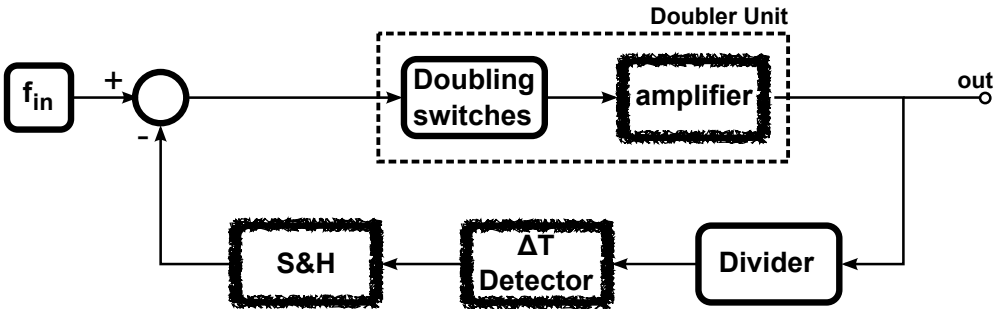


Figure 5.6: System model indicating dominant noise sources.

The reason for the amplifier to be expected as a dominant noise source is because it essentially fulfills the same role as a reference buffer in classical clocking circuits. As discussed in Chapter 2 in the PLL system the reference buffer

[4] in 'SpectreRF' this is called edge-to-edge jitter, J_{ee}^2

[5] Strictly spoken, the variance of absolute jitter is directly related to its own power spectrum. However, in [13] it is assumed that the spectral density of absolute jitter is the same as the spectral density of the phase.

accounts for 70% of the total noise. A reference buffer as such is still needed to obtain a clock signal with steep edges from a slow sine wave. The sample and hold circuit is expected to account for a significant amount of noise due to the on-resistance in combination with the hold capacitors that give kT/C noise.

First an estimation of the noise sources that are assumed white are given. These sources include the thermal noise from (Fig. 5.7):

- Drain resistors of the differential pair.
- Transistors of the differential pair.
- Transistors of second amplifier stage.
- Current mirror load of second amplifier stage
- Tail current source of integrator.
- On-resistors in sample-and-hold circuit (kT/C noise).

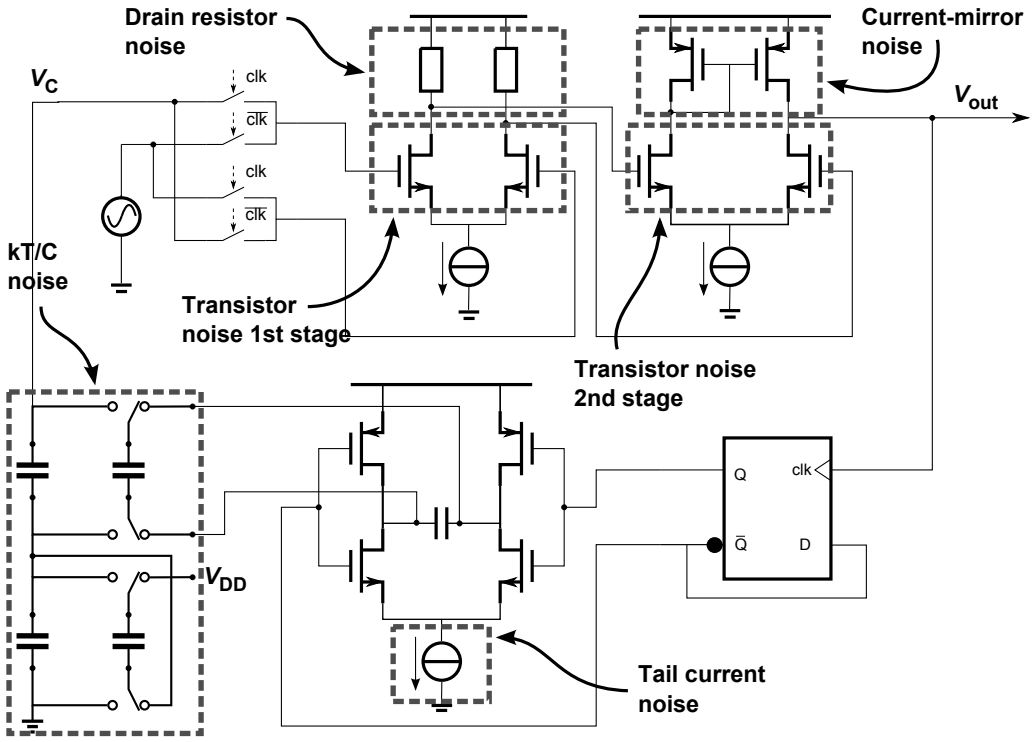


Figure 5.7: Circuit overview indicating dominant noise sources.

Table 5.1 shows the parameters as used in a first test design.

parameters	1st amp. stage	2nd amp. stage	integrator	sample-and-hold
Rd [ohm]	600	$11k$		
ro [ohm]	850	$8.5k$		
gm [ohm^{-1}]	$12m$	800μ	620μ	
I_{tail} [A]	$1m$	100μ	100μ	
C_i [F]			$50p$	
C_h [F]				$10p$
Noise Bandwidth [Hz]	$1G$	$3G$		

Table 5.1: Parameter values first test design.

Drain resistor noise
The noise contributions of both drain resistors in the first amplifier stage can be estimated by knowing there spectral densities. The one-sided PSD of a resistor is

$$\overline{I_{n,Rd}^2} = 4kT/Rd. \tag{5.4}$$

The total noise power contributed by the drain resistor to the output node V_{out} can be stated as $\overline{V_{out,Rd}^2} = 4kT/Rd \cdot (Rd//ro)^2 \cdot Av_2^2 \cdot f_{NB}$. Where Av_2 is the gain of the second amplifier stage and f_{NB} is the bandwidth of the noise. For the drain resistor vale as shown in Table 5.1 the total noise power at the output of the buffer stage is approximately $\overline{V_{out,Rd}^2} = 4kT/600 \cdot (600//850)^2 \cdot 4^2 \cdot 1 \times 10^9 \approx 5 \times 10^{-8}\text{V}^2/\text{Hz}$. This can be converted to jitter by dividing the latter number by the slew rate at node V_{out}. The total jitter is $\tau_{rms}^2 = 4e-8/(630 \times 10^6)^2 \approx 1.25 \times 10^{-25}\text{sec}^2$. The noise to carrier ratio $\mathcal{L}$ can be found using the following relation (where 5.2 is used)

$$\mathcal{L} = 2\pi^2 f_{out} \tau_{rms}^2. \tag{5.5}$$

Finally, the two drain resistors in the first amplifier stage contribute $10log(2 \cdot (2\pi^2 \cdot 40 \times 10^6 \cdot 1.25 \times 10^{-25})) \approx$ **-157dBc/Hz**.

Transistor thermal noise (1st stage)
The same approach can be used for estimating the thermal noise contribution of both transistors in the first amplifier stage. The spectral density of the thermal noise of a transistor is

$$\overline{I_{n,T}^2} = 4kT\gamma gm. \tag{5.6}$$

The total thermal noise power contributed by the transistors to output node V_{out} is then $\overline{V_{out,T1}^2} = 4kT\gamma gm \cdot (Rd//ro)^2 \cdot Av_2^2 \cdot f_{NB} = 4kT(2/3) \cdot 12 \times 10^{-3} \cdot (600//850)^2 \cdot 4^2 \cdot 1 \times 10^9 \approx 2.5 \times 10^{-7}\text{V}^2/\text{Hz}$. Converting to jitter gives $\tau_{rms}^2 = 2.5 \times 10^{-7}/(630 \times 10^6)^2 \approx 6.3 \times 10^{-25}\text{sec}^2$. Thus, based on (5.5), the two transistors in the first amplifier stage contribute $10log(2 \cdot (2\pi^2 \cdot 40 \times 10^6 \cdot 6.3 \times 10^{-25})) \approx$ **-150dBc/Hz**.

Transistor thermal noise (2nd stage)
The spectral density of the transistors in the 2nd stage as well as the current mirror transistors can be estimated using (5.6). A first estimation of the thermal noise contribution from each transistor in the second stage to its output is $\overline{V_{out,T2}^2} = 4kT\gamma gm \cdot (Rd//ro)^2 \cdot f_{NB} = 4kT(2/3) \cdot 800 \times 10^{-6} \cdot (8.5 \times 10^3//11 \times 10^3)^2 \cdot 3 \times 10^9 \approx 6 \times 10^{-7}\text{V}^2/\text{Hz}$. Converting to jitter gives $\tau_{rms}^2 = 6 \times$

$10^{-7}/(630\times10^6)^2 \approx 1.5\times10^{-24}\text{sec}^2$. Thus, based on (5.5), the four transistors in the second amplifier stage contribute $10log(4\cdot(2\pi^2\cdot40\times10^6\cdot1.5\times10^{-24}))\approx$ **-143dBc/Hz**. A simulation has been carried to verify the noise contribution from both stages which is shown in Fig. 5.8.

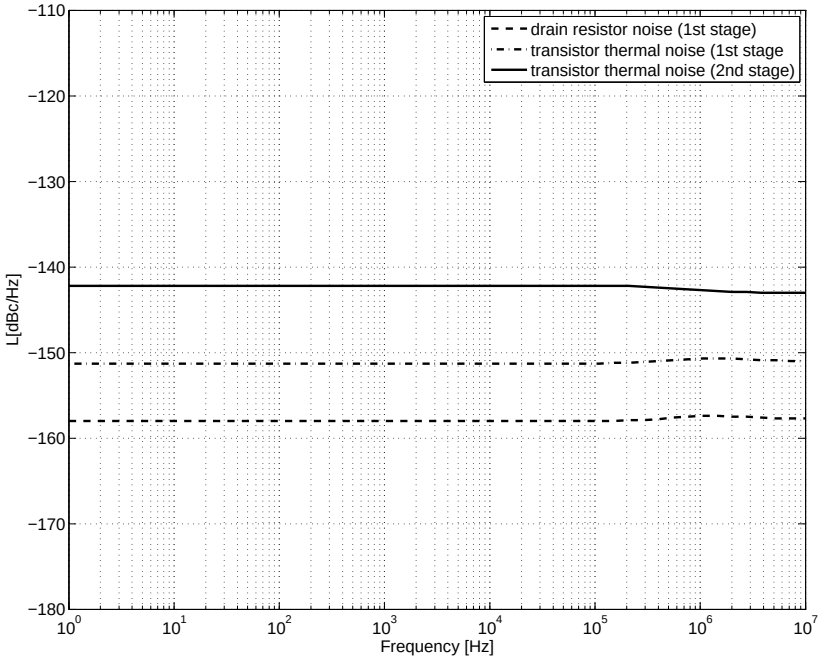


Figure 5.8: Simulation of thermal noise in 1st and 2nd stage.

Integrator tail current source

The noise floor contribution from the integrator circuit is dominated by the thermal noise from the tail current source transistor. The white noise from the current source appears as integrated noise at the input of the buffer circuit and therefore needs a more elaborate analysis to estimate its contribution to the output. Again the thermal noise from the transistor can be estimated using (5.6). This noise is then integrated by the integration circuit and flat by the drain-source resistance in the low frequency region. This is illustrated with a simulation in Fig. 5.9

The noise floor of the open loop can be estimated by $\overline{V^2_{out,Ti}} = 4kT\gamma gm\cdot(Rds)^2\cdot Av^2_{1,2} = 4kT(2/3)\cdot620\times10^{-6}\cdot(175\times10^3)^2\cdot15^2\approx7\times10^{-11}\text{V}^2/\text{Hz}$. Converting to jitter and next express in terms of phase noise using (5.1) gives $10log(((2\pi^2(40\times10^6)^2)/(630\times10^6))\cdot17\times10^{-11})\approx$ -113 dBc/Hz. After the flat region the noise rolls off with 20dB/dec. From the analysis in Chapter 4 can be derived that from the output of integrator circuit to the output of the 2nd buffer stage the loop exhibits a high-pass behavior. This means for the noise contribution from the integrator that it remains flat until the loop bandwidth, after which it will roll off again with 20dB/dec. In Fig. 5.9 it can be seen that at this point the noise decreased with approximately 30dB, which gives a noise

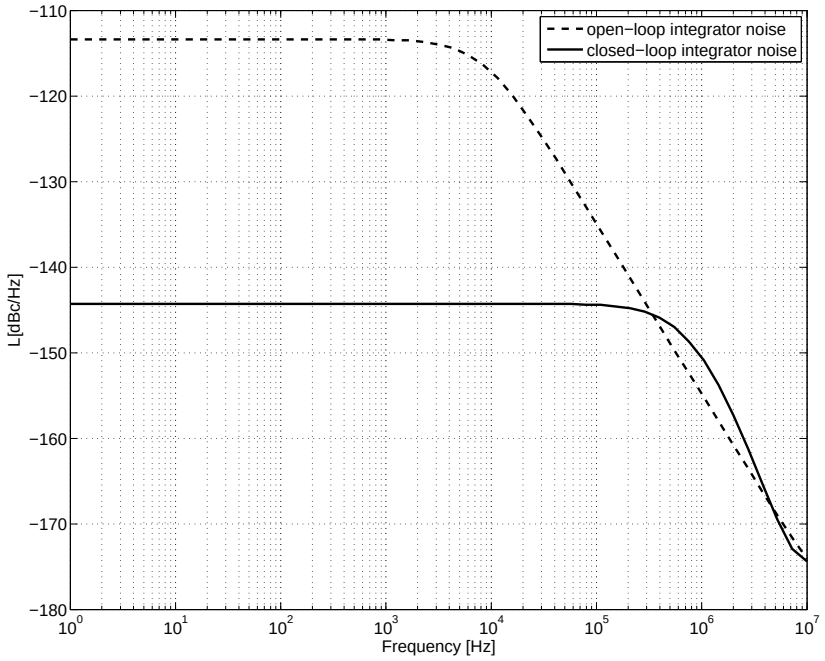


Figure 5.9: Simulation integrator thermal noise.

floor of approximately **-143 dBc/Hz**.

Sample-and-hold circuit

The output noise of a track-and-hold circuit is essentially the noise of the on-resistance of the track-and-hold switch. The noise is then shaped by the transfer function of the track-and-hold circuit at its on state. This is simply a low-pass filter with transfer function

$$H_{th}(s) = \frac{1}{R_{on}C_h s + 1}. \tag{5.7}$$

The spectral density of the track-and-hold then becomes

$$S_{th}(f) = S_{R_{on}} \cdot |H_{th}(s)|^2 \tag{5.8}$$

$$S_{th}(f) = 4kTR_{on}\frac{1}{(2\pi R_{on}C_h f)^2 + 1}. \tag{5.9}$$

The total noise power is found by integrating the power spectral density

$$P_{n,th} = \int_0^\infty \frac{4kTR_{on}}{(2\pi R_{on}C_h f)^2 + 1}\, df. \tag{5.10}$$

$$P_{n,th} = \frac{2kT}{\pi C_H} tan^{-1}(2\pi R_{on}C_h f)\Big|_{f=0}^{f=\infty}. \tag{5.11}$$

$$P_{n,th} = \frac{kT}{C_h}. \tag{5.12}$$

The total thermal noise power contributed by the sample-and-hold circuit to output node V_{out} can be estimated as $2 \cdot (kT/C_h) \cdot Av_{1,2}^2 = 2 \cdot (kT/10 \times 10^{-12}) \cdot 15^2 \approx 9 \times 10^{-8} \mathrm{V}^2/\mathrm{Hz}$. Converting to jitter gives $\tau_{rms}^2 = 9 \times 10^{-8}/(630 \times 10^6)^2 \approx 2 \times 10^{-25} \mathrm{sec}^2$. Finally, when using (5.5), the sample-and-hold stage contributes $10log(4 \cdot (2\pi^2 \cdot 40 \times 10^6 \cdot 2 \times 10^{-25})) \approx$ **-158dBc/Hz**. This noise is however shaped by the loop in the same manner as it did for the noise from the integrator circuit.

The noise coming from the sample-and-hold circuit is considered white at the input of the buffer circuit and is therefore shaped by the high-pass behavior. Fig. 5.10 shows a simulation of the total noise of the sample-and-hold circuit contributed to the output.

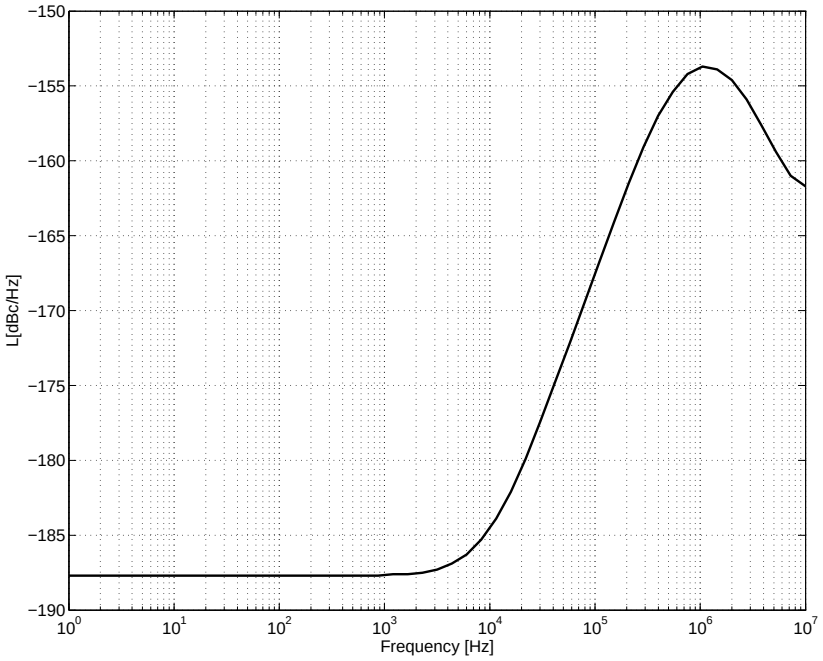


Figure 5.10: Simulation KT/C noise shaped by the loop.

5.3.1 Achieved Performance vs. Requested Performance

What is left is to draw conclusions on the noise estimation of the foregoing section. To this end, the noise estimations are summarized in Table 5.2.

As can be seen the achieved performance with a first circuit implementation is 12dB worse than the target specification. There is however roughly 3mW power budget left, which can be used to scale the amplifier stages and the integrator circuit. A first approximation is to scale the amplifier stages and

	Phase Noise	Power Dissipation
1st Stage	-149dBc/Hz	1.2mW
2nd Stage	-143dBc/Hz	0.12mW
Integrator	-143dBc/Hz	0.12mW
sample-and-hold	-158dBc/Hz	
Achieved Total	-139dBc/Hz	1.44mW
Required	-151dBc/Hz	4.2mW

Table 5.2: Achieved Performance vs. Requested Performance.

the integrator circuit such that they each contribute -156dBc/Hz. The first stage would have to have 6dB better phase noise performance. This means that 4 times more power has to be spent which comes down to a total of 4.8mW. Both 2nd amplifier stage and integrator would have to win 13dB, for which they each have to spend 20 times more power. Summing up the power dissipation would give a total power dissipation of roughly 10mW.

5.4 Summary

The noise analysis in this section shows how noise can be estimated and simulated when it has a cyclostationary behavior. An analysis has been made by estimating the most dominant noise sources and verifying them with simulation results. A first circuit implementation does not achieve the required specifications, leaving a gap of 12dB. This could be overcome by scaling the amplifier stage and the integrator circuit. This however would mean that more than twice the available power has to be spent.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

This work examined the feasibility of a low power and low noise CMOS Frequency Doubler in CMOS IC-technology. Based on the feasibility study on a PLL, the following conclusions can be drawn:

- A Figure-of-Merit (FoM) is used to give a measure of quality for a PLL design. It has been shown that with the given specifications, a PLL design would have such stringent jitter demands that its FoM would require to be almost 10 dB better than state-of-art PLL's.
- The feasibility of a PLL solution is assessed when using an high frequency LC oscillator, and divide its output frequency. To this end, a state-of-the-art PLL design is investigated with a FoM of almost -250dB. Even with this state-of-the-art design it has been shown that the in-band phase noise is a difficult demand to meet, given its power budget.
- The same PLL design shows that the dominant noise source is the reference buffer which accounts for 70% of the total noise contribution. This indicates that there is not much headroom next to the reference buffer. For a demand of -151dBc/Hz this gives that other noise sources apart from the buffer cannot add more than $10^{(-151/10)\cdot 0.3} \approx$ -156dBc/Hz.

Next to a PLL, an alternative has been examined which relies on passing through the edges of the clean reference crystal. This alternative method has partly been chosen based on the outcome of the PLL study and partly out of curiosity. It would be useful to know if an alternative Doubler solution, with essentially only a reference buffer in its signal path, would be feasible within the given specifications. Based on the study of this method and implementation on circuit level, the following conclusions can be drawn:

- An alternative doubler method is proposed: the Dual-Edge Doubler. By making use of both rising and falling edges of the incoming reference frequency and combining them into both rising edges, a doubled frequency can be obtained.

- The idea is analyzed and drawbacks with scenarios of possible error sources are sketched. As far as been investigated, all sources of error can be modelled as adjacent period jitter or duty-cycle error. This means that the adjacent periods of the doubled frequency are not equal to each other. Adjacent period jitter leads to unwanted spurious tones at reference frequency offsets of the carrier.

- To sufficiently reduce the spurious tones, a correction method can be applied which relies on charging and discharging a capacitor during two successive clock cycles of the output frequency.

- A detailed system analysis of the circuit design has been carried out. Its behavior is quantified and the predictions are compared to circuit simulations that show good agreement to each other. It shows that adjacent period jitter can be reduced to well beyond 140ps, which meets the spurious noise demands.

- Noise analysis shows that main noise contributors are the 1st and 2nd amplifier stage (as expected, since this is essentially the buffer stage) and the integrator circuit. In a first circuit implementation the total noise contribution of the analyzed circuits give a noise floor of -139dBc/hz with 1.44mW power dissipation.

- When using width scaling, the total noise can be reduced to the target specification of -151dBc/Hz, for which roughly 10mW would be needed.

6.2 Recommendations

Based on the work presented in this thesis some recommendations can be made for possible future work:

- Implementation of the clock circuitry that controls the Doubler switches have not yet been discussed. The switches have to switch somewhere near the topple-point of the sinusoid, in between the two edges. The clock could therefore, most rudimentary, be derived from the sinusoid itself by using the topple-points as trigger moments. As far as can be overseen, the timing of this clock is non-critical.

- Difference in rise and fall times of the divider output could degrade the loop its ability to reduce adjacent period jitter. This problem can however be overcome by implementing the divider as current-mode-logic which ensures equal rise and fall times.

- Speed limitations could be analyzed if the circuit is to be extended for higher frequencies. The circuit shows proper functioning for 20 - 50MHz input range, but is not further analyzed in terms of limitations.

- Noise contribution of the divider has to be analyzed.

- Effect on-resistance of the on system performance has to be analyzed. These include: thermal noise contribution from on-resistance to output, and influence of charge injection.

- The circuit implementation is not optimized for noise. This can be done for the buffer circuit without changing the dynamics of the loop. The noise contribution from the integrator has to be more carefully analyzed. The noise could possibly be reduced by increasing its swing. Increasing the swing will however give more loop gain which could drive the system in instability. This gives a direct trade-off between noise and loop dynamics.

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